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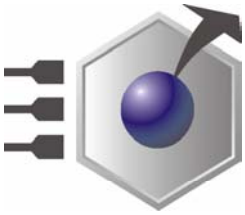

EuroTecH

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CPU-1232: Additional Counters / timers

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ABOUT THIS MANUAL

This application note contains information for using additional Counters / Timers on the CPU-1232

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Conventions

The following table lists conventions used throughout this guide.

Icon	Notice Type	Description
	Information note	Important features or instructions
	Warning	Information to alert you to potential damage to a program, system or device or potential personal injury

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Chapter 1 Introduction

The CPU1232 has three extra 8254 compatible 16bit Timer Counters available, apart from standard AT timers. They are referred here as COUNTER0, COUNTER1 and COUNTER2.

The chip used is the UPD71054 from NEC semiconductor.

The Clock input for the three timers has a fixed internal 1MHz frequency.

If enabled (see later on I/O map) an interrupt can be generated on a timer output pin rising edge. More than one timer can be enabled at any time, and the IRQ sources can be OR'ed together. The interrupt is routed to ISA IRQ10. If unused the internal glue logic lets the driver interrupt in tri-state and IRQ10 can be assigned to another device.

Please note that gate inputs are hardwired to a high logic level.

Due to this limitation the three counters can be programmed to work only in some operating modes as shown below:

Mode	Description	Availability
0	Interrupt on End of count	Available
1	GATE re-triggerable One-Shot	NOT Available
2	Rate generator	Available
3	Square Wave generator	Available
4	Software Triggered Mode	Available
5	Hardware Triggered Strobe	NOT Available

For further information refer to the following data books:

- UPD71054: "NEC- Microprocessor and peripherals"
- 8253 & 8254: "INTEL- Microprocessor and peripheral"

Chapter 2 Accessing the UPD71054

The three timers can be accessed trough the registers of internal glue logic mapped in I/O space

The relevant registers are shown in this chapter

I/O Port 118h, E1001_IRQ_TIMER

Reset Value: xxx

Bit	Mode	Name	Description
2	Read / Write	E1001_IRQ_TIMER0	Enable the third channel to send an interrupt 0: Disable counter 2 interrupt 1: Enable counter 2 interrupt
1	Read / Write	E1001_IRQ_TIMER1	Enable the second channel to send an interrupt 0: Disable counter 1 interrupt 1: Enable counter 1 interrupt
0	Read / Write	E1001_IRQ_TIMER2	Enable the first channel to send an interrupt 0: Disable counter 0 interrupt 1: Enable counter 0 interrupt

Note: In order to get an interrupt from a timer you must first enable the bit 0 address 119h

I/O Port 119h, E1001_DEVICE_CTRL

Reset Value: x10

Bit #	Mode	Name	Description
0	Read / Write	E1001_CTRL_TIMER	Enable timer device to give an interrupt. 0: Interrupt generation disabled 1: interrupt generation enabled The interrupt generated is IRQ10.

I/O Port 11Ch to 11Fh, E1001_TIMER_DATA_CNTL

Bit	Mode	Name	Description
7:0	Read / Write	Not Applicable	Reserved. These are reserved as Timer 71054 registers. 11Ch: Counter 0 data register 11Dh: Counter 1 data register 11Eh: Counter 3 data register 11Fh: Control word register

Chapter 3 Example application

Together with this document you will find a simple application that shows how to program the counters.
The source code written in the “C” programming language and can be found in the file “TTIM.C”
The executable file for MS-DOS is “TTIMER.EXE”. Just run TTIMER from DOS prompt.
Be sure that IRQ10 is not used for other devices (for internal devices please check the BIOS).

The application first programs the COUNTER0 in Mode 0(interrupt on End Of Count) Binary Count to get an End Of Count after 12ms and waits for an interrupt from IRQ10 line. Then does the same thing for COUNTER1 and COUNTER2.
For further information refer to C source code.

Warning:
In order to get correct results, you must disable the SMI interface on CPU1232.
The code needed to disable and restore SMI interface is shown below:

```
#define GX1_INDEX 0x22
#define GX1_DATA  0x23
void SMI_restore(unsigned char mask)
{
      disable();                    //Disable interrupts
      outportb(GX1_INDEX,0xC1);
      outportb(GX1_DATA,mask);
      enable();
}

char SMI_disable(void)
{
 unsigned char gx1_tmp;
 disable();                         //Disable interrupts
 outportb(GX1_INDEX,0xc1);
 gx1_tmp=inportb(GX1_DATA);
 outportb(GX1_INDEX,0xC1);
 outportb(GX1_DATA,0);
 enable();
 return gx1_tmp;
 }
```

Related Documents

For further information on the CPU-1232 please refer to the following

Manuals:

- CPU-1232: User Manual.

Application Notes:

- An-0006, CPU1232 IOMAP
- An-0027, CPU1232 Memory, IO, IRQ and DMA
- An-0031, CPU1232 Cable set
- An-0035, Soft Power Management
- An-0048, Expansion Socket

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