VMEbus SBC with 2nd Generation Intel® Core i7™

CPU 71-15

- Legacy VME or VME64 compatible
- 2nd Generation Core i7
- MIL-STD-810F versions
- Convection and Conduction-cooled
- RTM available for rear I/O support

CPU 71-15 shown without heat sink

FEATURES

VME Compatible – Tundra Universe IID PCI-VMEbus interface provides VME64 compatibility and backward compatibility with older VME backplanes.

High Perfomance and Low Power – Dual core processing at less than 25W typical power consumption enables cool operation at extended temperature.

Gigabit Ethernet – Three Ethernet ports are provided, one on the front and two on the rear, VITA 31.1 compatible.

MIL-STD Versions – The CPU 71-15 is offered in versions that support wedge locks for high shock and vibration immunity, and conduction-cooling. Conformal coating is available for all versions.

- Defense
- Homeland Security

- AerospaceIndustrial
- Industrial
 Tremenortation
- Transportation

The CPU 71-15 is a high performance Single Board Computer (SBC) based on the VMEbus 6U form factor. The CPU 71-15 is offered in both convection cooled and ruggedized conduction cooled variants, meeting the needs of numerous commercial and military applications requiring maximum processing power, low power consumption, and small physical footprint.

At the heart of the CPU-71-15 is an Intel® 2nd Generation Core™ i7 ULV Sandy Bridge Processor and a QM67 Cougar Point Platform Controller Hub (PCH). These two devices form the central processing backbone of the design. With a dual-channel memory controller integrated in the processor, the CPU-71-15 supports up to 8 GBytes of DDR3 SDRAM running at up to 1333 MHz.

The CPU-71-15 supports two PMC and one optional XMC sites: the on-board XMC site is connected to the Core i7 CPU by one x8 gen 2 PCle link; the two PMC sites are implemented with a PCle to PCl bridge (PLX8112) connected to the QM67 PCH with a x1 PCle link. The VME interface to the backplane is implemented with the Universe IID PCI-VMEbus interface controller.

The CPU-71-15 offers both front panel and P2/P0 Ethernet ports: an Intel 82579 10/100/1000BaseT Ethernet controller is routed to an RJ45 interface on the front panel access, while an 82571EB dual 10/100/1000 BaseT, provides two additional Gigabit Ethernet ports routed to either P2 or P0 in compliance with the VITA 31.1 Ethernet backplane network. Three RS232 ports and an LPT1 port are also routed to P2.

Operating system support is provided for VxWorks, Linux, and Windows.



CPU 71-15

Specifications

System Architecture

CPU

- INTEL® CORE™ 17-2655LE / 2.2GHz, 25W
- INTEL® CORE™ 17-2610UE / 1.5GHz, 17W

CHIPSET

MOBILE INTEL®QM67

PLATFORM CONTROLLER HUB (PCH)

- INTEL® COUGAR POINT QM67 PLATFORM CONTROLLER HUB
- PCI EXPRESS BASE SPECIFICATION, REVISION 2.0
- ENHANCED DMA CONTROLLER, INTERRUPT CONTROLLER, AND TIMER FUNCTIONS
- INTEGRATED 3G SERIAL ATA HOST CONTROLLERS WITH INDEPENDENT DMA
- USB HOST INTERFACE WITH SUPPORT FOR EIGHT USB PORTS
- System Management Bus (SMBus) Specification, Version 2.0 with additional support for on-board I2C devices
- SUPPORTS INTEL® RAPID STORAGE TECHNOLOGY
- SUPPORTS INTEL® VIRTUALIZATION TECHNOLOGY FOR DIRECTED I/O
- SUPPORTS BUFFERED MODE GENERATING EXTRA CLOCKS FROM A CLOCK CHIP
- LVDS
- ANALOG DISPLAY PORT (VGA)
- FIRMWARE HUB (FWH) INTERFACE

DRAM

4 OR 8 GB DDR3-ECC SOLDERED MEMORY

ETHERNET

82579 BASET SINGLE CHANNEL VIA X4 PCIE FROM PCH 82571EB BASET DUAL CHANNEL VIA X4 PCIE FROM PCH

SMSC LPC4M10S7 SUPER I/O

- DUAL COM PORTS SUPPORT RS-232
- KYBD/MOUSE
- LPT INTERFACE

NON-VOLATILE STORAGE

- ON-BOARD CONNECTOR FOR BOOTABLE HIGH-SPPED CFAST
- 64MBIT EEPROM ON SPI BUS FOR BIOS

PMC/XMC

- x8 PCI Express Bus from Processor to XMC site 1 (JN4 I/O TP PO)
- \bullet 32-bit, 33 MHz PCI bus available to both PMC/XMC sites

VME REAR I/O

- PO VITA 31.1 COMPATIBLE DUAL GB ETHERNET, PMC/XMC SITE 1 I/O, x1 SATA 3G
- P2 COM 1,2 & 3; LPT, x2 10/100Base-T (alternate Ethernet
- ROUTING OF ETHERNET NORMALLY ROUTED TO PO), PMC SITE 2 I/O

FRONT PANEL I/O

PS/2 kybd/mouse, 10/100/1000 BaseT (RJ45 connnector), 5x USB 2.0 (type A connectors), 2x stacked SATA connectors, LVDS Molex 53015-12110 12-pin connector, and high density DB15 VGA connector Optional PMC/XMC I/O access

MISCELLANEOUS

• ON-BOARD TEMPERATURE MONITORING VIA SMBUS

Power Consumption

- Estimated +5V @ 5A (typ)
- TOTAL POWER: 25W (TYP) BASED UPON 2610UE PROCESSOR
- Actual power depends on CPU 71-15 product configuration and XMC and USB loads
 - (Power consumption values subject to change without notice)

FORM Factor

• 6U VMEBUS

RUGGED/CONDUCTION-COOLED

- AVAILABLE IN CONDUCTION-OOLED VERSIONS
- Optional wedge locks provide high shock and vibration immunity per MIL-STD-810F
- CONVECTION AND CONDUCTION-COOLED VERSIONS HAVE CONFORMAL COATING AS AN OPTION
- Available in standard and extended operating tempearture range

BIOS

• PHOENIX SECURECORE TIANO UEFI



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VMEbus SBC with 2nd Generation Intel® Core i7™

Block Diagram





VMEbus SBC with 2nd Generation Intel® Core™

Specifications

CPU 71-15



PARAMETER	CONDITION	RANGE	COMMENT	
Temperature	Operating	-0°C to +70°C (-40° to +85° C versions available)	Clock throttling can be implemented for wider temperature ranges	
	Storage	-50°C to +85°C		
Humidity	Operating	20 to 95% non-condensing	±4% relative humidity, per MIL-STD-810F	
	Storage	0 to 100% non-condensing		
Altitude		Unlimited		
Vibration	Sine	10g peak 15-2 kHz	All levels based on a sweep duration of 10 minutes per axis, each of three mutually perpendicular axes. Qualification testing is displacement limited below 44 Hz.	
	Random	0.1 g2/Hz 15-2 kHz (14.1 grms)	60 minutes per axis each of three mutually perpendicular axes.	
	Shock	40 g peak	Three hits per direction per axis, 1/2 sine + terminal peak sawtooth, 11mS (total 36 hits).	



I/0	FRONT PANEL	VME PO*	VME P2		
Ethernet (10/100BaseT)			2 (when no PO populated)		
1 Gigabit Ethernet (10/100/1000BaseT)	1	2 (VITA 31.1)			
PMC/XMC I/O	Optional	Site 1 PMC/XMC	Site 2 PMC only		
Serial ATA 3G	2	1			
USB 2.0	5				
LVDS	1				
SVGA	1				
PS2 Keyboard/Mouse	1				
RS-232			3		
LPT			1		
* PO connector is optional					

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