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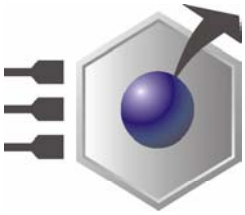

EuroTecH

An0051

CPU-1850; TFT Digital Interface

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ABOUT THIS MANUAL

This application note contains information about how to connect a TFT/LCD Digital Interface to the CPU-1850.

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NOTICE

Conventions

The following table lists conventions used throughout this guide.

Icon	Notice Type	Description
	**Information note**	Important features or instructions
	**Warning**	Information to alert you to potential damage to a program, system or device or potential personal injury

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Contents

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Chapter 1 CPU-1850 TFT Digital Interface

This brief application note contains information about using the CPU-1850 TFT digital interface. The goal is to help users connecting TFT-LCD panels to the CPU-1850.

TFT Digital Interface Overview

The CPU-1850 allows you to connect various models of LCD-TFT panels via the J2 connector. For some TFT/LCD you will require a LVDS receiver like the ACS-9030 Adapter. Table 1 shows the supported LCD-TFT video resolutions:

Table 1. LCD-TFT video resolutions (*)

Resolution	Color Bit	Refresh Rate (Hz)
640x480	18	60
640x480	24	60
800x600	18	60
800x600	24	60
1024x768	18	60
1024x768	24	60

(*) This list is not meant to be a complete list of all the possible supported TFT video

For further information about other or new LCD-TFT flat panels supported, please contact the Eurotech Customer Support Service.

J2 CPU TFT Digital Interface Connector

The TFT digital interface available on the CPU-1850 J2 connector is a LVDS interface, which complies with Open LDI specifications for digital displays.
J2 is a double row 10 x 2 pin with 2.0 mm step connector.

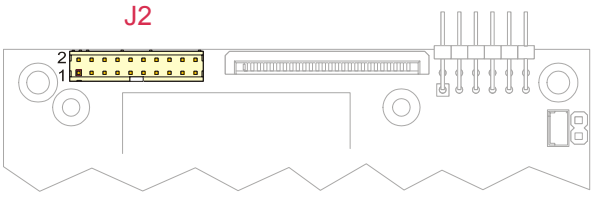

Figure 1. CPU-1850 TFT connector

TFT Digital Interface Pin Out

Table 2 describes the signals of the J2 TFT Digital Interface connector:

Table 2. J2 TFT Digital Interface connector pinout

Pin	Signal	Function
1	GND	Ground
2	CLK1+	Positive LVDS differential clock output
3	CLK1-	Negative LVDS differential clock output
4	GND	Ground
5	A0+	Positive LVDS differential data output
6	A0-	Negative LVDS differential data output
7	GND	Ground
8	A1+	Positive LVDS differential data output
9	A1-	Negative LVDS differential data output
10	GND	Ground
11	A2+	Positive LVDS differential data output
12	A1-	Negative LVDS differential data output
13	GND	Ground
14	A3+	Positive LVDS differential data output
15	A3-	Negative LVDS differential data output
16	LVDSON	This output signal enable the LVDS receiver
17	SDAT	I2C signal for expansion devices
18	SCLK	I2C signal for expansion devices
19	GND	Ground
20	N.C.	

For further information about the physical relationships of the J2 connector please refer to the Figure 1.

This information is intended to help the user to properly realize the cable used to connect the Digital interface of the CPU-1850 with the TFT LCD Panel selected or the ACS-9030 Module.

Reducing the cable length will reduce the possible interference seen on the TFT LCD digital signals.

Color bit mapped to LVDS Outputs

Figure 2 shows the map of the color bit on the LVDS Channels. Note that here the Open LDI bit number is used, so bit 6 and 7 are the less significant bit.

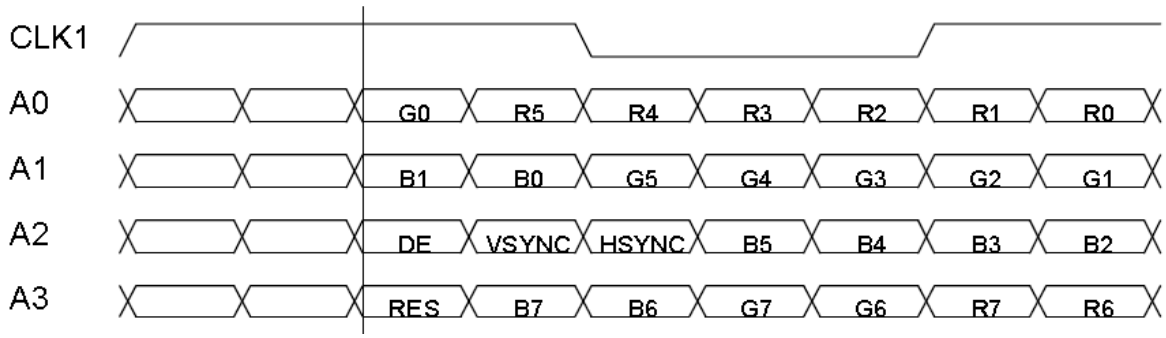

Figure 2. Map of the color bit on the LVDS Channels

Table 3 lists the Bit Number Mappings:

Table 3. Bit Number Mappings

18 bits per pixel bit number	24 bits per pixel bit number	OpenLDI bit number
5	7	5
4	6	4
3	5	3
2	4	2
1	3	1
0	2	0
	1	7
	0	6

Chapter 2 The Eurotech LVDS receiver (ACS-9030)

The module ACS-9030 is a Eurotech LVDS receiver that is composed by the following parts:

- National 90CF386 LVDS receiver
- Power switch for the TFT/LCD power supply
- Power switch for the DC/AC CCFL inverter
- Power sequencer circuit
- Brightness control (optional)
- Multiple output connectors for different LCD connectors

How to connect the ACS-9030

Figure 3 shows a schematic draw of the Eurotech ACS-9030 LVDS receiver.

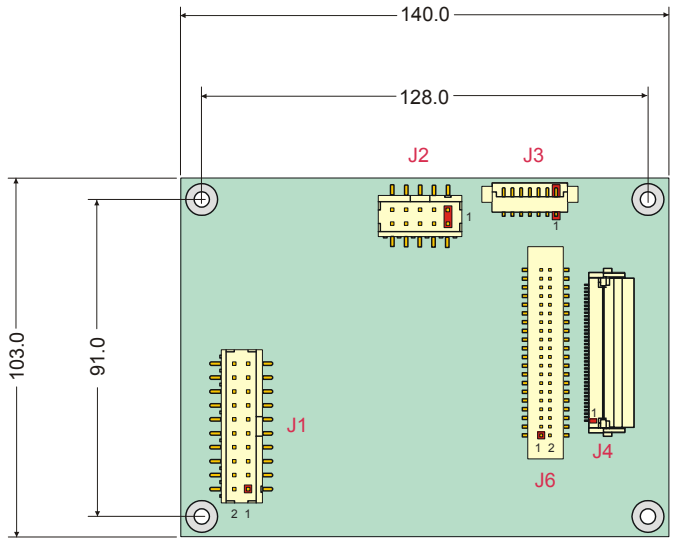

Figure 3. The Eurotech ACS-9030 LVDS receiver

Table 4 lists the name of the connectors and their function.

Table 4. ACS-9030 Connector Functions

Connector	Function
J1	LVDS Input from Transmitter. Connect to Cpu1850 on connector J2
J2	Power input from Power Supply. Connect to Power supply with proper cable
J3	Power Out to DC/AC CCFL Inverter Connect to DC/AC CCFL Inverter with proper cable
J4	LCD Digital interface output – ZIF 40 Pin Can be connected to LCD via FFC
J5	LCD Digital interface output – BTB 41 Pin Can be plugged into LCD
J6	LCD Digital interface output – Crimp wire 40 Pin Can be connect to LCD via proper cable

J1 Connector

J1 is a double row 10 x 2 pin with 2 mm step connector, FCI Part number 98424-G52-20A.

Table 5. ACS-9030 J1 Connector pin out

Pin	Signal	Function
1	GND	Ground
2	CLK1+	Positive LVDS differential clock input
3	CLK1-	Negative LVDS differential clock input
4	GND	Ground
5	A0+	Positive LVDS differential data input
6	A0-	Negative LVDS differential data input
7	GND	Ground
8	A1+	Positive LVDS differential data input
9	A1-	Negative LVDS differential data input
10	GND	Ground
11	A2+	Positive LVDS differential data input
12	A1-	Negative LVDS differential data input
13	GND	Ground
14	A3+	Positive LVDS differential data input
15	A3-	Negative LVDS differential data input
16	LVDSON	This input signal enable the LVDS receiver
17	SDAT	I2C signal for expansion devices
18	SCLK	I2C signal for expansion devices
19	GND	Ground
20	N.C.	

J2 Connector

J2 is a double row 10 x 2 pin with 2 mm step connector, FCI part number 98424-G52-10A

Table 6. ACS-9030 J2 Connector pin out

Pin	Signal	Function
1	+5V_PWR	+5V Input used for module circuits. Must be connected to +5V DC.
2	PWRLCD	+3.3V or +5V input for LCD power supply. Connect the proper voltage as required by LCD
3	+3.3V_OUT	3.3V output – can be connected to pin 2 and can supply up to 200mA for LCD. This voltage comes from a linear regulator and can be used to supply the LCD-TFT as long as the voltage matches and the current requirement is under 200mA
4	PWRBLIGHT	+5V or +12V input for DC/AC CCFL Inverter. Connect the proper voltage as required by inverter.
5	GND	Common Ground

J3 Connector

J3 is a Single row 7Pin Male, Molex Part number 53261-0790.
This pin-out nearly matches the pin-out of some inverters like TDK CXA-P1212B-WJL.

Table 7. ACS-9030 J3 Connector pin out

Pin	Signal	Function
1,2	VCC_BLIGHT	Timing-controller enabled Positive voltage from PWRBLIGHT
3,4	GND	Common Ground
5,6	+5V_PWR	+5V output for DC/AC CCFL Inverter control
7	BLIGHT_VBR	Variable output for brightness control (option). Otherwise NC.

J4 Connector

J4 is a ZIF for FFC cable 40 pin, AVX-ELCO Part number 04 6240 040 003800.
The other side of FFC cable can be plugged into LCD/TFT.
Otherwise the adapter E3204 can be connected on the other side of FFC cable to plug into a LCD type HITACHI tx31d30vc1caa 800X600 18bit.

Table 8. ACS-9030 J4 Connector pin out

Pin	Function		Pin	Function
1	GND_1		21	G4
2	CLK		22	NC_1
3	GND_2		23	G5
4	HSYNC		24	G6
5	VSYNC		25	G7
6	GND_3		26	NC_2
7	R0		27	B0
8	R1		28	B1
9	R2		29	B2
10	R3		30	B3
11	R4		31	B4
12	GND_4		32	GND_5
13	R5		33	B5
14	R6		34	B6
15	R7		35	B7
16	NC_3		36	DE
17	G0		37	GP0
18	G1		38	VCC_LCD
19	G2		39	VCC_LCD
20	G3		40	GP1

The digital TFT interface signals of ACS-9030 J4 are described in table 9:

Table 9. ACS-9030 J4 Connector signals

SIGNAL NAME	Description	Electrical Characteristics
Dot Clock	Pixel Port Clock Dot Clock is the pixel dot clock output. It clocks the pixel data.	TTL 8mA V_{HMAX} = 3.3V
HSYNC	Flat Panel Horizontal Sync Flat Panel Horizontal Sync establishes the line rate and horizontal Retrace interval for a TFT display.	TTL 8mA V_{HMAX} = 3.3V
VSYNC	Flat Panel Vertical Sync Flat Panel Vertical Sync establishes the screen refresh rate and vertical retrace interval for a TFT display.	TTL 8mA V_{HMAX} = 3.3V
DE	This is a data valid signal	TTL 8mA V_{HMAX} = 3.3V
RED[7:0]	Graphics Red Pixel Data Bus This bus drives graphics pixel data synchronous to the Dot Clock output. Bit 7 is MSB, Bit 0 is LSB .	TTL 8mA V_{HMAX} = 3.3V
GREEN[7:0]	Graphics Green Pixel Data Bus This bus drives graphics pixel data synchronous to the Dot Clock output. Bit 7 is MSB, Bit 0 is LSB .	TTL 8mA V_{HMAX} = 3.3V
BLUE[7:0]	Graphics Blue Pixel Data Bus This bus drives graphics pixel data synchronous to the Dot Clock output. Bit 7 is MSB, Bit 0 is LSB .	TTL 8mA V_{HMAX} = 3.3V
GP0, GP1	General purpose output	TTL 8mA V_{HMAX} = 3.3V
VCC_LCD	Power output for LCD power supply. Timing-controller enabled Positive voltage from PWRLCD	+3.3V or +5V based on PWRLCD
GND	Ground	Ground

J5 Connector

J5 is a Board to board connector 41 pin, HIROSE Part number DF9B-41S-1V.
Can be plugged into a LCD type HITACHI tx31d30vc1caa 800X600 18bit.
For a signal description refer to J4 Signal Description.

Table 10. ACS-9030 J5 Connector pin out

Pin	Function		Pin	Function
1	GND_1		21	G2
2	CLK		22	GND_10
3	GND_2		23	G3
4	HSYNC		24	G4
5	VSYNC		25	G5
6	GND_3		26	GND_11
7	GND_4		27	GND_12
8	GND_5		28	GND_13
9	R0		29	B0
10	R1		30	B1
11	R2		31	B2
12	GND_6		32	GND_14
13	R3		33	B3
14	R4		34	B4
15	R5		35	B5
16	GND_7		36	GND_15
17	GND_8		37	DE
18	GND_9		38	GP1
19	G0		39	PWR_1
20	G1		40	PWR_2
			41	GP0

J6 Connector

J6 is a Board to wire connector 40 pin, HIROSE Part number DF13-40DP-1.25V.
For a signal description refer to J4 Signal Description.

Table 11. ACS-9030 J6 Connector pin out

Pin	Signal		Pin	Signal
1	GND_1		21	G4
2	CLK		22	NC_1
3	GND_2		23	G5
4	HSYNC		24	G6
5	VSYNC		25	G7
6	GND_3		26	NC_2
7	R0		27	B0
8	R1		28	B1
9	R2		29	B2
10	R3		30	B3
11	R4		31	B4
12	GND_4		32	GND_5
13	R5		33	B5
14	R6		34	B6
15	R7		35	B7
16	NC_3		36	DE
17	G0		37	GP0
18	G1		38	VCC_LCD
19	G2		39	VCC_LCD
20	G3		40	GP1

Chapter 3 BIOS Setup

To enable the TFT Digital Interface functionality you have to properly configure the BIOS settings. This section is intended to show you the BIOS settings you should modify to properly control the LCD-TFT. For further information on how to use the BIOS functionalities please refer to the CPU-1850 Manual.

CPU-1850 BIOS Menu

After entering BIOS setup by pressing the F2 Key during the initial boot sequence, select the Flat Panel menu using cursors and you will be prompted by the following menu:

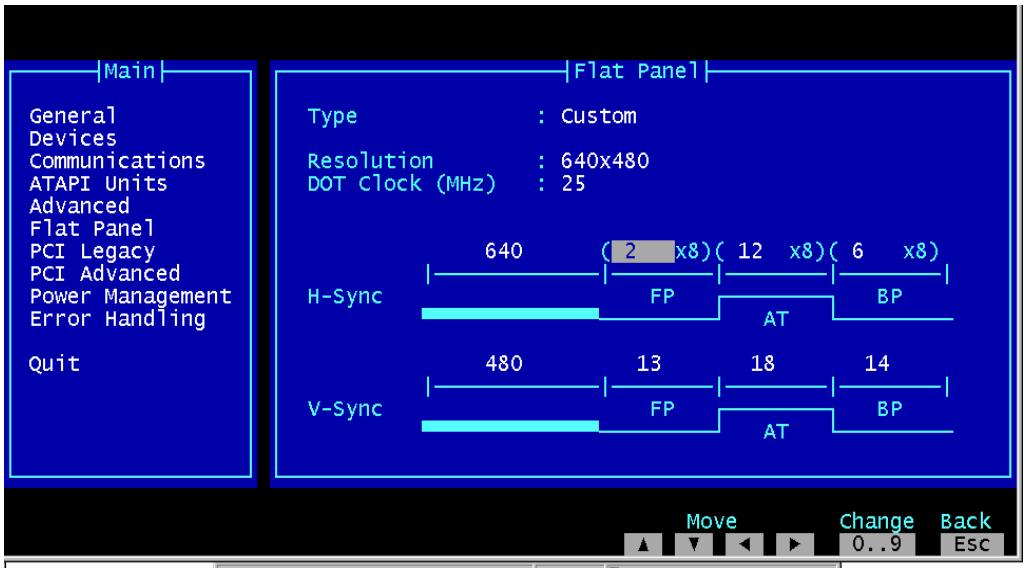

Figure 4. BIOS setup - Flat Panel section

CPU-1850 BIOS Flat Panel parameters

Table 12 gives a brief description of the BIOS setup parameters and their default values:

Field	Description		Default Value
Type	Disabled	Disabled	Disabled
	Custom	Custom parameters	
	Hitachi 800x600 (38MHz)		
	LG 800x600 (38MHz)		
	NEC 800x600 (38MHz)		
	Sharp 800x600 (40MHz)		
Resolution	640x480	Select the proper graphical resolution	640x480
	800x600		
	1024x768		
Dot Clock (MHz)	Dot Clock Frequency in MHz		0
HSync FP	Front Porch - Horizontal Sync		0
HSync AT	Active Time - Horizontal Sync		0
HSync BP	Back Porch - Horizontal Sync		0
VSync FP	Front Porch - Vertical Sync		0
VSync AT	Active Time - Vertical Sync		0
VSync BP	Back Porch - Vertical Sync		0

Table 12. BIOS Flat Panel section Options

To properly enter the parameters you will have to analyze the information contained in the TFT-LCD Data Sheet you want to connect to the CPU-1850 and insert the data for the various fields.

Sometimes when you connect both the CRT connector and the TFT interface what happens is that the image shown into the CRT is rescaled and shifted because the parameters inserted for the TFT interface modify the video settings.

Defining CPU-1850 BIOS parameters

To enter the proper parameters into the Flat Panel BIOS settings you have to refer to the TFT-LCD Datasheet. Table 13 shows an example of a timing table referred to a 640x480 TFT-LCD.

Parameter		Symbol	Min.	Typ.	Max.	Unit	Remarks
CLK	Frequency	1/tc	21.0	25.175	29.0	MHz	39.722 ns (Typ.)
	Duty	tch/tc	0.4	0.5	0.6	–	–
	Rise, fall	tcrf	–	–	10	ns	–
Hsync	Period	th	30.0	31.778	33.6	µs	31.469 kHz (Typ.)
			–	800	–	CLK	
	Display period	thd		640		CLK	–
	Front-porch	thf		16		CLK	Fixed timing mode
			2	16	–	CLK	DE mode
	Pulse width	thp*	10	96	–	CLK	Fixed timing mode
			10	96	–	CLK	DE mode
	Back-porch	thb*	4	48	–	CLK	Fixed timing mode
			4	48	–	CLK	DE mode
	thp + thb*			144		CLK	Fixed timing mode
			14	144	–	CLK	DE mode
	CLK-Hsync timing	thch	12	–	–	ns	–
	Hsync-CLK timing	thcs	8	–	–	ns	–
	Hsync-Vsync timing	tvh	1	–	–	CLK	1CLK = 39.722 ns (Typ.)
	Vsync-Hsync timing	tvs	30	–	–	ns	–
	Rise, fall	thrf	–	–	10	ns	–
Vsync	Period	tv	16.1	16.683	17.2	ms	59.94 Hz (Typ.)
			–	525	–	H	
	Display period	tvd		480		H	–
	Front-porch	tvf		12		H	Fixed timing mode
			1	12	–	H	DE mode
	Pulse width	tvp*	1	2	–	H	Fixed timing mode
			1	2	–	H	DE mode
	Back-porch	tvb*	4	31	–	H	Fixed timing mode
			4	31	–	H	DE mode
	tvp + tvb*			33		H	Fixed timing mode
			5	33	–	H	DE mode
	Rise, fall		–	–	10	ns	–
DATA R0 - R5 G0 - G5 B0 - B5	CLK-DATA timing	tds	8	–	–	ns	–
	DATA-CLK timing	tdh	12	–	–	ns	–
	Rise, fall	tdrf	–	–	10	ns	–
DE	DE-CLK timing	tes	8	–	–	ns	DE mode
	CLK-DE timing	teh	12	–	–	ns	
	Rise, fall	terf	–	–	10	ns	

Table 13. Timing Characteristic Example for a TFT-LCD

The following instructions would be an example for showing how to define the values to enter into the Flat Panel BIOS setup referring to the Table 13 timing characteristics.

BIOS Field	BIOS Value	Notes
Type	Custom	We would enter custom parameters
Resolution	640x480	Obtained from the TFT-LCD Data Sheet, this is a characteristic.
Dot Clock (MHz)	25	Referring Table 13 CLK (1/Tc) Typical value. The reported value 25.175MHz is approximated to 25Mhz
HSync FP	2	Referring Table 13 HSync Front Porch (thf) Typical value. The reported value 16CLK. So the value you've to enter the BIOS is 2 to obtain 16 = (2 x 8)
HSync AT	12	Referring Table 13 HSync Pulse width (thp*) Typical value. The reported value 96CLK. The value you've to enter the BIOS is 12 to obtain 96 = (12 x 8)
HSync BP	6	Referring Table 13 HSync Pulse Back-porch (thb*) Typical value. The reported value 48CLK. The value you've to enter the BIOS is 6 to obtain 48 = (6 x 8)
VSync FP	12	Referring Table 13 VSync Front Porch (tvf) Typical value. The reported value 12CLK.
VSync AT	2	Referring Table 13 VSync Pulse width (tvp*) Typical value. The reported value 2 H.
VSync BP	31	Referring Table 13 VSync Back Porch (thb*) Typical value. The reported value 31CLK.

Table 14. Flat Panel BIOS parameters

Timings Diagrams

The followings images show you a graphical mode for represent timing data. This information is not represented in the same graphical order shown in the Flat Panel BIOS setup, but the contents are the same.

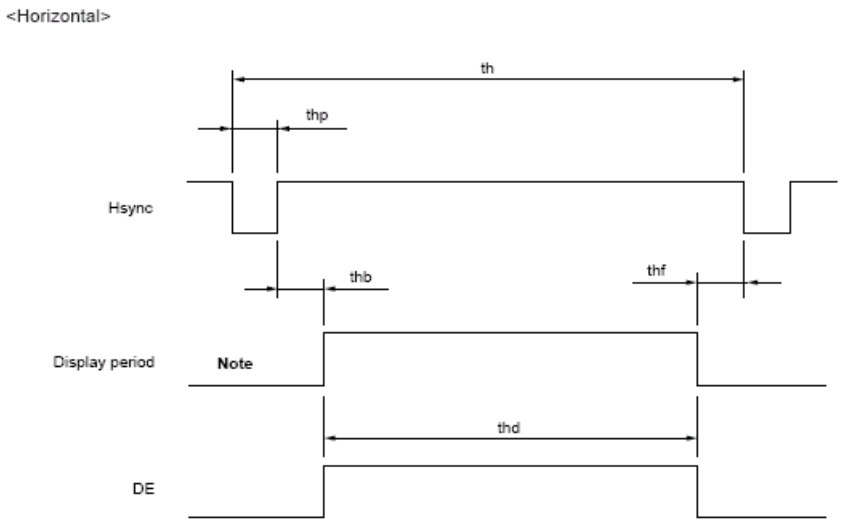

Figure 5. Timing Diagram Horizontal Mode

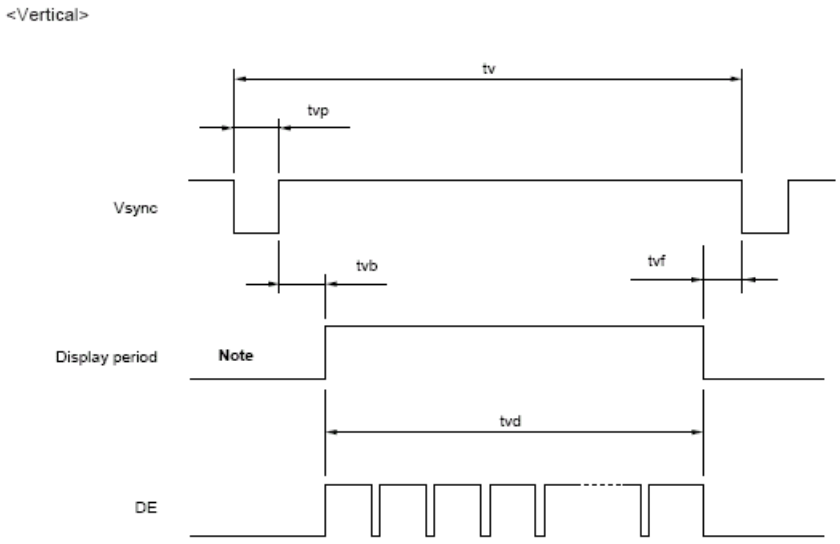

Figure 6. Timing Diagram Vertical Mode

The previous Figures may be useful for graphically verifying that the parameters entered into the BIOS comply with the TFT timing diagram.

Regarding the timings the following relations must be guaranteed:

Horizontal Sync. :

Period (th) = Display Period (thd) + Front Porch (thf) + Pulse Width (thp*) + Back Porch (thb*)

Vertical Sync. :

Period (tv) = Display Period (tvd) + Front Porch (tvf) + Pulse Width (tvp*) + Back Porch (tvb*)

Practically, referring to Table 13 and to Table 14, the results are:

Horizontal Sync: 800 = 640 + 16 + 96 + 48

Vertical Sync: 525 = 480 + 12 + 31 + 2

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Chapter 4 Connecting the TFT LCD to the CPU-1850

This section contains a brief checklist for connecting a TFT LCD to the CPU-1850.

- First of all download all the information about the TFT-LCD module and its CCFL inverter you selected;
- Verify that the resolution of your TFT panel is compatible and supported with the resolutions reported in Table 1 of this Application note;
- Carefully read the TFT-LCD data sheet you have selected in particular the Electrical Characteristics that must be compatible with the electrical interface of the CPU-1850 TFT LCD interface or the ACS-9030 module.
- If you have to connect a TFT/LCD Flat panel with a traditional C-Mos interface, then you can make the following simple connections using the ACS-9030:
  - Connect J2 from CPU-1850 to J1 of ACS-9030
  - Connect a power supply to J2 of ACS-9030; connect +5V or +3.3V on PWRLCD pin (2) as needed by LCD-TFT; connect +5V or +12V on PWRBLIGHT pin (4) as needed by CCFL inverter. Do not connect pin 3 or make a short between pin 2 and 3 only if the LCD require a +3.3V and less than 250 mA. Warning: pin 3 of J2 is an output; do not connect unless you are sure about what you are doing. Finally connect a common GND on pin 5. Refer to the description of J2 for more information.
  - Connect J3 from ACS9030 to the CCFL inverter. Connection is pin-to-pin for TDK CXA-P1212B-WJL, except the brightness (pin 7), which is an option on ACS-9030 module and pin 6 which have to be left unconnected.
  - Connect the LCD-TFT to J4, J5 or J6 whichever best meets your needs. Maybe you need a specific cable or the E3204 mechanical adapter for HITACHI tx31d30vc1caa.
  - If you have to connect a TFT/LCD Flat Panel with built-in LVDS receiver, then you don't need the LVDS receiver of the ACS-9030 module. Check the color mapping scheme and then write a table with the connections between Cpu1850 and the TFT-LCD, you can use the ACS-9030 for the timings of power management.
  - You have to refer to the TFT-LCD Input Signal timing Data Sheet section to detect the parameters you need to insert into the CPU-1850 BIOS Flat Panel section and calculate its as described in the BIOS Setup. Maybe a predefined LCD will work fine with your LCD, even if it is a different vendor or part number. Resolution is the most important parameter.
  - First connect the system carefully verifying the cable connections, the BIOS settings and all the information to prevent erroneous damages to the system.
- After you have verified the information you can power up the system verifying that all the data is displayed properly on the TFT LCD module. Try some graphical test programs to detect the functionality of the images.