







CTR-1472; Multiple MPEG4 Stacking Capability

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ABOUT THIS MANUAL

This application note contains information about the CTR-1472 PC/104+ stacking capabilities.



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Conventions

The following table lists conventions used throughout this application note.

lcon	Notice Type	Description
i	Information note	Important features or instructions
	Warning	Information to alert you to potential damage to a program, system or device or potential personal injury

Mode of the register:

R/W: Read and write register.

RO: Read only register.

W: Meaning of the register when written.

R: Meaning of the register when read.

Name ranges:

A name followed by a range in brackets represents a range of logically related entities. For example Name [0:2]

Hex Number: Hexadecimal numbers are represented with an "h" suffix. (For example 11Ch)

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Chapter 1 CTR-1472 Multiple Stacking Capability

This brief application note is intended to help users to make multiple CTR-1472 PC/104+ boards stacked together function correctly, providing some undocumented information necessary when you want to stack four boards. This document is not intended to describe the PC/104+ Specification contents, for this we suggest to refer to the bibliography.

CTR-1472 MPEG4 Hardware stacking

The CTR-1472 is a PC/104+ MPEG4 hardware compression board that operates in a bus master mode during the hardware compression.

PC/104+ Stacking

To assemble the CTR-1472 boards together and make it work on the PC/104+ architecture you need to identify the boards in a different way assigning different slot numbers for each board.

For this kind of activity we suggest you refer to the CTR-1472 board manual where this information is provided. In Table 1 we summarize the jumper settings for slot assignment.

JP#	Туре	Function			Default
		JP1	JP2	PCI Selection Slot:	
	2 nin	Closed	Closed	Slot0	JP1 and
JP1-2	JP1-2 2 pin	Open	Closed	Slot1	JP2
Jump	jumper	Closed	Open	Slot2	Closed
		Open	Open	Slot3	

 Table 1.
 CTR-1472, Jumper Slot selection settings

Figure 1 shows an example of the CTR-1472 stack assembly where, Assuming that the CPU is installed on the top of the stack, it illustrates how to stack the boards to increase the BUS performance, considering that the clock wires related to each slot selection are optimized depending on the bus length.

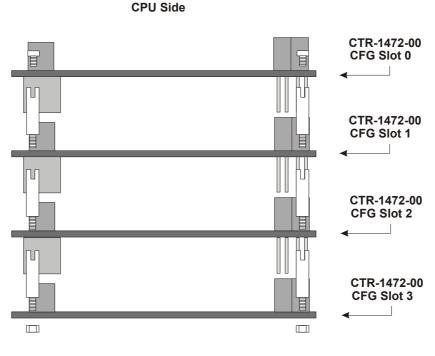


Figure 1. CTR-1472 Example Stack

PC/104+ Specification Version 1.X vs. V 2.0

In this section we focus on the main differences between the PC/104+ Specification Version 1.x and Version 2.0, which is the number of the supported Bus Master peripherals as summarized in the following table:

Specification	Number of PC/104+ Expansion Boards BUS Master Capable	
PC/104 + Vers. 1.X	3	
PC/104 + Vers. 2.0	4	

Table 2. PC/104+ Specification

The main difference is that the PC/104+ Specification Version 2.0 introduces two additional signal lines (REQ3 and GNT3) for managing the capability of BUS master on the fourth board stacked.

For a detailed description of the PC/104+ Specification we suggest to refer to the bibliography.



Looking at Table 2 we understand that if you want to use a stack of four CTR-1472 (which operates in a BUS Master mode during compression) it is not possible to use a CPU that is not PC/104+ Version 2.0 compliant.



CTR-1472 MPEG4 PC/104+ v2.0 Schematic solution

The CTR-1472, for supporting the compatibility with the PC/104+ Version 1.X Specification, has a dedicated electronic circuitry which allow users to redirect the signals REQ and GNT to accomplish both the PC/104+ Version 1.X and Version 2.0 making some jumper resistors modification as illustrated in the Figure 2.

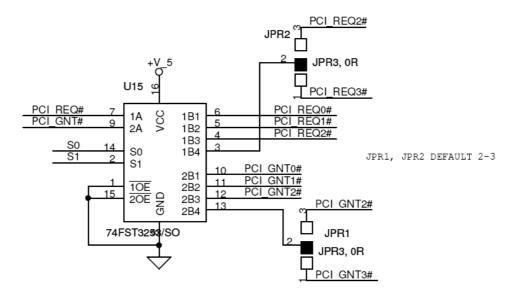


Figure 2. CTR-1472 PC/104+ v2.0 Schematic settings

The following table illustrates the jumper settings and related resistor settings to accomplish the PC/104+ Version 1.X or 2.0.

Specification	JPR1	JPR2
PC/104 + Vers. 2.0	PCI_REQ3# 1-2	PCI_GNT3# 1-2
PC/104 + Vers. 1.X	PCI_REQ2# 2-3 (Default)	PCI_GNT2# 2-3 (Default)

Table 3. CTR-1472 PC/104+ V1.1 or V2.0 selection

In general it is not common to use four CTR-1472 boards stacked together, for this reason the default setting of jumpers JPR1 and JPR2 are configured for supporting the PC/104+ Version 1.X Specification, in this case you don't have to mind on the CPU PC/104+ version.

In this application note we analyze the case for using four CTR-1472 boards stacked.





Stacking four CTR-1472 MPEG4 boards

Following is a summery of the requirements for using four CTR-1472 MPEG4 boards as described in the previous paragraphs.

- Verify that you're using a CPU that is PC/104+ version 2.0 compliant
- Configure each CTR-1472 slot referring to Table 1 for verifying the jumper settings
- Modify the assigned slot 3 CTR-1472 to operate with GNT3 and REQ3 signals as described in Table 3
- Assemble the four CTR-1472 in the stack as illustrate in Figure 1
- Power up the system enter the BIOS settings and enable the BUS Master capability for the CTR-1472 PC/104+ peripherals
- Boot your O.S. and verify that the boards' resources are properly detected.
- Using the proper driver for the specific O.S. try to compress simultaneously from each board



CTR-1472 MPEG4 Assembly drawing

To easily detect the position of the JPR1 and JPR2 jumper solder resistors the assembly drawing of the CTR-1472 are showed in the following pictures.

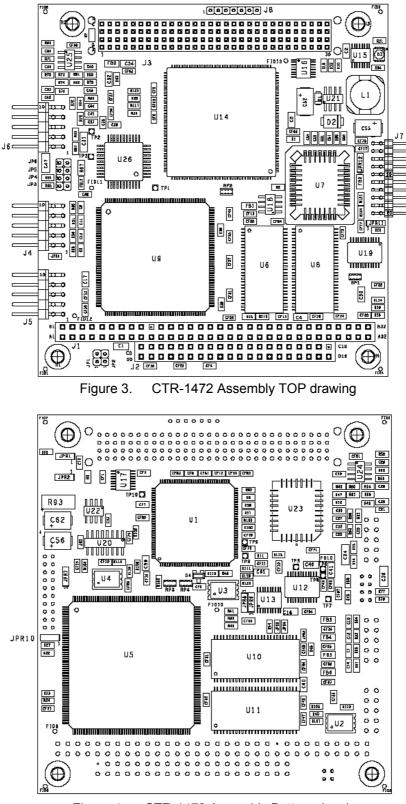


Figure 4. CTR-1472 Assembly Bottom drawing



CPU BIOS Settings

In general Eurotech CPU PC/104+ boards have a BIOS Menu where it is possible to modify the setting to allow user to select the Bus Master capability. Enabling the Bus Master capability the CTR-1472 boards are capable of driving in master mode the PCI bus.

The following figure shows typical settings used in a system with four CTR-1472 modules stacked with a CPU-1451 processor board.

Main General Devices Communications Primary ATAPI Advanced PCI Advanced Flat Panel Error Handling Quit	PCI Advance ISA Irq for PCI INT_A (Share 2) ISA Irq for PCI INT_B (Share 2) ISA Irq for PCI INT_C (Share 2) ISA Irq for PCI INT_D (Share 2) Bus Master (Devices) Latency Time (Devices) Force CardBus Internal Clock	: 10 : 10 : 10 : 10 : Enabled : 32
	Move	<mark>Change Back</mark> PgUp/- PgDn/+ Esc

Figure 5. CPU-1451 BIOS V. 4.x.x PCI Devices

If user requires he can modify the interrupt assignments to make the boards interrupt independently.



Related Documents

For more information please refer to the specific CPU user manual. PC/104+ Specification v 1.1 PC/104+ Specification v 2.0 http://www.eurotech.it www.pc104.org www.pc104.org

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