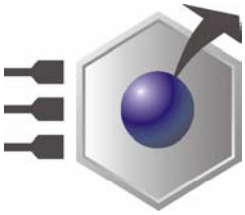
EmbeddedDNA®



EuroTecH

THE COMPLETE EMBEDDED PC SOLUTION

An0041

CPU-1450; Memory I/O IRQ DMA Maps

Rev. 0.1

Oct. 2004

Via J. Linussio 1
33020 AMARO (UD)
ITALY
Phone: +39 0433 485 411
Fax: +39 0433 485 499

web: http://www.eurotech.it
e-mail: mailto:sales@eurotech.it

NOTICE

Conventions

The following table lists conventions used throughout this guide.

Icon	Notice Type	Description
	**Information note**	Important features or instructions
	**Warning**	Information to alert you to potential damage to a program, system or device or potential personal injury

Mode of the register:
R/W: Read and write register.
RO : Read only register.
W : Meaning of the register when written.
R : Meaning of the register when read.

Name ranges:
A name followed by a range in brackets, for example Name[0:2], represent a range of logically related entities.

Hex Number:
Hexadecimal numbers are represented with a ‘h’ suffix. (for example 11Ch)

(This page is intentionally left blank.)

Contents

(This page is intentionally left blank.)

Foreword

In the following tables, this Application note describes, the Memory map, the I/O map, the IRQ map, the DMA map and the PCI Configuration space for the CPU-1450.

Tables

Memory space

Start address (Hex)	End Address (Hex)	Area Amount	Device name and/or function	Physical Device or Bus selected
00000	9FFFF	640Kbyte	Main system area	Onboard SDram
A0000	BFFFF	128Kbyte	Video buffer Area	Onboard VGA Memory
C0000	CFFFF	64Kbyte	Video BIOS Area	Onboard VGA Memory
D0000	DFFFF	64Kbyte	Free area	
E0000	FFFFF	32Kbyte	BIOS Area	Onboard Flash
100000	[1]	XMbyte	System Memory Used by operating system	Onboard SDram
4000_0000	7FFF_FFFF		PCI prefetchable memory area	
8000_0000	FDFF_FFFF		PCI no prefetchable memory area	
Top of Memory[2]	4GB	XMbyte	PCI memory area	PCI bus
FE00_0000	FECF_FFFF		APIC configuration space	Onboard Flash
FED0_0000	FEDF_FFFF		Reserved	
FEE0_0000	FEEF_FFFF		APIC configuration space	Onboard Flash
FFE0_0000	FFFF_FFFF		High BIOS Area	

[1] The End Address depends on the amount of RAM Memory Size you've installed into the board. The RAM block is continuous starting from the Start Address.
[2] For the same reason of the previous point the start address of the PCI bus free area depends on the RAMmemory size installed into the board.

I/O map

Start address (Hex)	End Address (Hex)	Area Amount	Device name and/or function
0000	001F	32 byte	8237 DMA controller 1 registers.
0020	0021	2 byte	8259 Interrupt controller 1 registers.
0022	002D	12 byte	RESERVED
002E	002E	1 byte	IO_Super IO_Index
002F	002F	1 byte	IO_ Super IO _Data
0030	003D	14 byte	8259 Interrupt controller
0040	0043	4 byte	8254 Timer/Counter registers. 1
004E	004F	2 byte	Forwarded to LPC
0050	0053	3 byte	Timer/Counter
0060	0060	1 byte	8742 KeyBoard Controller - IO_8742_DATA
0061	0061	1 byte	System Control - IO_PORT_B
0062	0063	2 byte	Forwarded to LPC
0064	0064	1 byte	8742 KeyBoard Controller - IO_8742_STS
0065	0067	3 byte	Forwarded to LPC
0070	0070	1 byte	CMOS/Real Time Clock – IO_CMOS_Index
0071	0071	1 byte	CMOS/Real Time Clock – IO_CMOS_Data
0072	0077	6 byte	RESERVED
0080	009F	32 byte	DMA controller
0100	0100	1 byte	Monitor Serial Port
0110	0110	1 byte	VP Link (for VP2000 program)
00A0	00A1	2 byte	8259 Interrupt controller
00A2	00BD	28 byte	RESERVED
00C0	00DF	32 byte	8237 DMA controller 2 registers. 1
00F0	00F0	1 byte	FERR#/IGNNE#/Interrupt
0170	0177	8 byte	IDE Controller2
01F0	01F7	8 byte	Primary IDE controller 1
0376	0376	1 byte	Secondary IDE controller 2
0378	037B	4 byte	LPT possible address or free
03E8	03EF	8 byte	COM possible address or free
03B0	03BB	12 byte	Vga
03C0	03DF	32 byte	Vga
03F6	03F6	1 byte	Primari IDE Controller1
03F8	03FF	8 byte	COM possible address or free
0481	048B	7 byte	DMA High Page registers.
04D0	04D1	2 byte	8259 Interrupt Edge/Level Select Register
0CF8	0CF8	1 byte	PCI Configuration Space - IO_PCI_Addr
0CF9	0CF9	1 byte	Reset Generator(Processor I/F) - PCI Configuration Space
0CFC	0CFC	1 byte	PCI Configuration Space - IO_PCI_Data

Start address (Hex)	End Address (Hex)	Area Amount	Device name and/or function
07000	07019	32 byte	National SUPER IO System Wakeup Ctrl
07008	07008	1 byte	IO_ Super IO _GPIOE_Port_0_DataOut[3]
07020	07020	1 byte	IO_SUPER IO_GPIO_Port_0_DataOut
07021	07021	1 byte	IO_SUPER IO_GPIO_Port_0_DataIn
07022	07022	1 byte	IO_SUPER IO_GPIO_Port_0_Event_Enable
07023	07023	1 byte	IO_SUPER IO_GPIO_Port_0_Event_Status
07024	07024	1 byte	IO_SUPER IO_GPIO_Port_1_DataOut
07025	07025	1 byte	IO_SUPER IO_GPIO_Port_1_DataIn
07026	07026	1 byte	IO_SUPER IO_GPIO_Port_1_Event_Enable
07027	07027	1 byte	IO_SUPER IO_GPIO_Port_1_Event_Status
07028	07028	1 byte	IO_SUPER IO_GPIO_Port_2_DataOut
07029	07029	1 byte	IO_SUPER IO_GPIO_Port_2_DataIn
0702A	0702°	1 byte	IO_SUPER IO_GPIO_Port_3_DataOut
0702B	0702B	1 byte	IO_SUPER IO_GPIO_Port_3_DataIn
0702C	0702C	1 byte	IO_SUPER IO_GPIO_Port_4_DataOut
0702D	0702D	1 byte	IO_SUPER IO_GPIO_Port_4_DataIn
0702E	0702E	1 byte	IO_SUPER IO_GPIO_Port_4_Event_Enable
0702F	0702F	1 byte	IO_SUPER IO_GPIO_Port_4_Event_Status
07030	07033	4 byte	National SUPER IO Watch Dog
07080	70BF	64 byte	ICH2 GPIO Base Address
070C0	070C0	1 byte	ICH2 SMBus Base Address

[3] IO_Super IO_GPIOE_Port_XX, IO_SUPER IO_GPIO_Port_XX_DataIn, IO_SUPER IO_GPIO_Port_XX_Event_Enable, IO_SUPER IO_GPIO_Port_XX_Event_Status registers are referred to the J15 GPIO connector not installed by default on CPU-1450.

IRQ assignment

Hardware IRQ	Assignment
0	System timer
1	Keyboard
2	Second programmable interrupt controller cascade
3	COM or LPT possible or free
4	COM or LPT possible or free
5	COM or LPT possible or free
6	Standard Floppy Disk controller
7	COM or LPT possible or free
8	Real Time Clock / Cmos
9	COM or LPT or Network Adapter possible or free
10	COM or LPT or Network Adapter possible or free
11	COM or LPT or Network Adapter possible or free
12	COM or LPT or Network Adapter or Mouse PS/2 possible or free
13	Reserved
14	Primary IDE controller
15	Free[4]

DMA assignment

Hardware DMA	Assignment	Physical source
0	LPT or free	ISA or LPT
1	LPT or free	ISA or LPT
2	Standard Floppy Disk controller	ISA
3	LPT or free	ISA or LPT
4	DMA controller Cascade	ISA or LPT
5	Free	ISA
6	Free	ISA
7	Free	ISA

The previous tables display the available I/O spaces and interrupts that can be used by devices. To avoid conflicts please check BIOS settings, space used or and custom interrupt settings.

[4] Note: In some Operating Systems (e.g. WinXP) INT 15 is not allowed.

PCI Configuration space

Bus	Dev	Function	Description
0	0	0	HostHub to DRAM controller
0	2	0	HostHub to graphic system
0	30	0	Hub Interface to PCI Bridge
0	31	1	PCI to LPC Bridge(includes: DMA, Timers, PIC , APIC, RTC, CPU I/F, Power management, System Management control,GPIO)
0	31	1	IDE Controller
0	31	2	USB Controller #1
0	31	3	SMBus Controller
0	31	4	USB Controller #2
0	31	5	AC'97 Audio Controller
1	0	X	Slot 0 PC104+ (if present)
1	1	X	Slot 1 PC104+ (if present)
1	2	X	Slot 2 PC104+ (if present)
1	3	X	Slot 3 PC104+ (if present)
1	6	0	PCI to ISA bridge
1	8	0	LAN Controller