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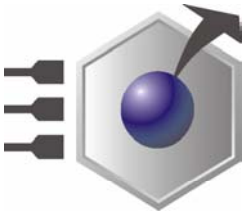

EuroTecH

THE COMPLETE EMBEDDED PC SOLUTION

An0039

CPU-1232; Soft power Management

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ABOUT THIS MANUAL

This application note contains information regarding the CPU-1232 Soft Power Management programming mode.

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NOTICE

Conventions

The following table lists conventions used throughout this guide.

Icon	Notice Type	Description
	**Information note**	Important features or instructions
	**Warning**	Information to alert you to potential damage to a program, system or device or potential personal injury

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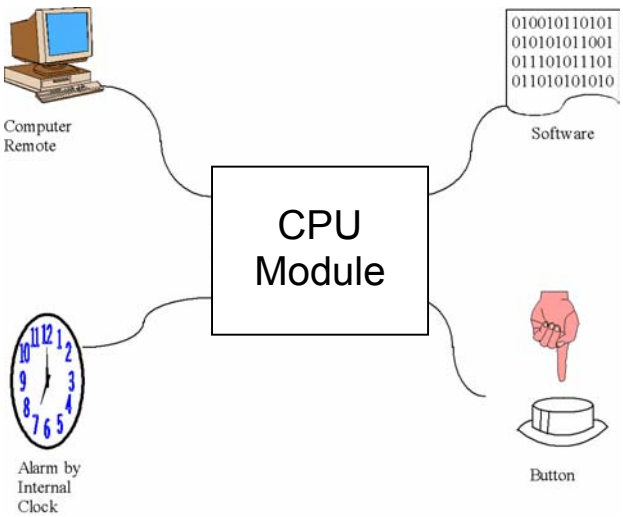
Chapter 1 The Soft Power Management

Soft power management (SPM) is a technique that allows users to put the CPU module into a low power mode (to decrease power consumption), while maintaining the ability to return to normal use, upon demand.

When the CPU-1232 module is powered off with the SPM, only a small portion of the board is supplied power. This part monitors system inputs, looking for wake-up events.

This low power mode can be activated through software or via a power button, whereas it can be deactivated from either the power button or through one of a number of wake-up events (i.e. receiving ringing signals from serial ports or from the network line, or an alarm at a predetermined time).

Table 1. Soft Power Management



The CPU-1232 module supports Advanced Configuration Power management Interface (ACPI), a standard for PCI power management of modern operating systems that enables Operating System Directed Power Management (OSPM) to achieve the most efficient power management. Besides the ACPI feature, the CPU-1232 module also supports remote wake-up (including Magic Packet). The CPU-1232 module is capable of

performing an internal reset whenever there is (auxiliary) power applied. Once the auxiliary power is on and the main power remains off, the CPU-1232 module is ready and is waiting for the Magic Packet* or other wake-up events.

Advantage and disadvantage

To use the SPM mode, the CPU-1232 module needs an ATX-like power supply with two supplies::

- A principal supply (VDD) that can be turned on and off by software.
- An auxiliary supply (5VSB) that is always present.

WARNING: Once the auxiliary power is on, the board is always supplied power so take special care in handling it.

Without an ATX-like power supply, the CPU-1232 module cannot work with SPM and the power keeps all of the board features on.

CPU-1232 SPM Connectors

This section is intended to allow user to find the connectors related to the SPM functionality. These are: the Auxiliary Power connector (which supplies power to the board), Multifunction connector, External Ring for wake-up, and the Ethernet connector.

Auxiliary Power Connector

One auxiliary power connector is available on the CPU-1232 module. J11 is a 6x2 pin connector with 2.54-mm step used to power the module when not powering via the PC/104-Plus bus.

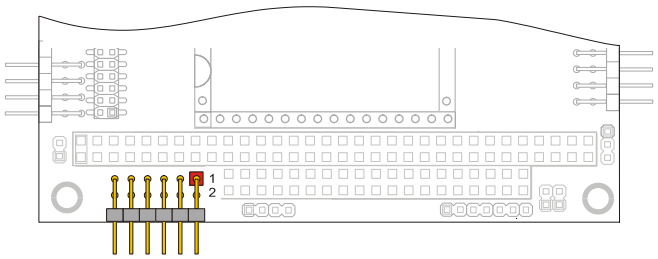


Figure 1. J11 Connector layout

Table 2. J11 Auxiliary Power Connector

Pin	Signal	Description
1	GND	Ground
2	VDD (+5VDC)	+5VDC signal
3	N.C.	Not connected
4	+12VDC	+12VDC signal

5	N.C.	Not connected
6	-12VDC	-12VDC signal
7	GND	Ground
8	VDD (+5VDC)	+5VDC signal
9	N.C.	Not connected
10	N.C.	Not connected
11	+5VSB	Always high (ATX only)
12	ATX ON	ATX Power on signal

For the SPM, the 5VSB must be provided at the pin11 of the J11 CPU-1232 connector.

To manage the ATX power on and off modes, the user should connect pin 12 ATX ON to the ATX Power on signal.

Multifunction connector

The J3 Multifunction connector is a 5x2 pin connector with 2.54-mm step, which may be used to connect an external push-button between J3 pin 10 and GND, to power the CPU-1232 module up and down.

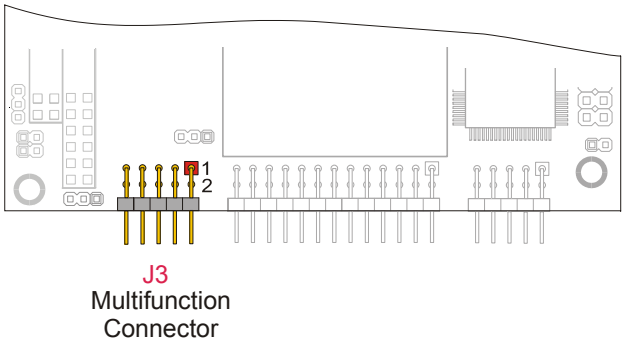


Figure 2. J3 Connector layout

Table 3. J3 Multifunction connector

Pin	Signal	Function
1	SPKR-	Speaker output
2	SPKR+	Speaker output (+5V)
3	RESET	External reset
4	WDTL	Watch dog timeout latch
5	KBD	Keyboard data
6	KBC	Keyboard clock
7	GND	Ground signal
8	KBP	Keyboard power (+5V)
9	BAT	External Battery input
10	P_B	External Power Button

External Ring for Wake-up

With this connector (2 pin, 2mm step) it is possible to wake up the system from an external ring.

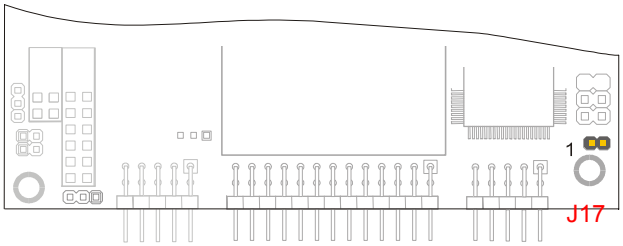


Figure 3. J17 Connector layout

The connector pinout is shown below:

Table 4. J17 nRINGING Connector

Pin	Signal	Description
1	EXTRING#	GP11
2	GND	Ground

Ethernet connector

The CPU-1232 integrates an Ethernet interface based on the Realtek RTL8139C chip, which is accessible via J18 Ethernet connector. Ethernet connector J18 is a 5x2 pin with 2.54-mm step. Refer to the following table for the Ethernet connector assignment.

Note: To establish a connection to Ethernet, the Ethernet Adapter should be plugged in between the CPU board (to the J18 connector) and the network cable.

It is shown below.

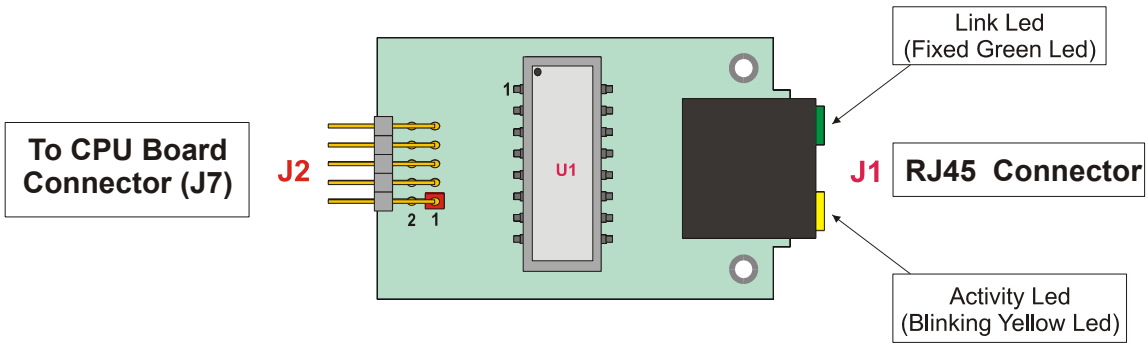


Figure 4. Ethernet Adapter

The green LED is fixed and signals proper connection of the module. The yellow LED blinks when there is activity (data IN/OUT) on the network connection. When the user enters the low power mode this LED functionality is not enabled.

With RJ-45 connectors, only twisted pair cables can be used.

Important Note. Connection to a 100BASE-TX hub for 100 Mbps operation requires Cat. 5 Unshielded Twisted-Pair (UTP) cable or Cat. 5 Shielded Twisted-Pair (STP) cable. The maximum length between the 100BASE-TX hub and the adapter is 100 meters. Connection to a 10BASE-T hub for 10 Mbps operation requires a Cat. 3, 4, 5 UTP cable or Cat. 5 STP cable. Recommended maximum cable length between CPU-1232 module and Ethernet adapter is 10 cm (4”)

The CPU-1232 module features a single-chip Fast Ethernet controller that provides 32-bit performance, 10/100Mbps auto-sensing, PCI bus master capability, and full compliance with IEEE 802.3u 100Base-T specifications and IEEE 802.3x Full Duplex Flow Control.

Electrical connections

In general, if the user desires to supply the CPU-1232 with an ATX power supply, following are the connections to make:

Table 5. CPU-1232 to ATX cable connections

J11 Aux PWR		Function	ATX	
Pin	Signal		Pin	Wire Color
1	GND	Ground	5	Black
2	VDD (+5VDC)	+5VDC signal	4	Red
3	N.C.	Not connected	--	N.C.
4	+12VDC	+12VDC signal	10	Yellow
5	N.C.	Not connected	--	N.C.
6	-12VDC	-12VDC signal	12	Blue
7	GND	Ground	15	Black
8	VDD (+5VDC)	+5VDC signal	6	Red
9	N.C.	Not connected	--	N.C.
10	N.C.	Not connected	--	N.C.
11	+5VSB	Always high (ATX only)	9	Purple
12	ATX ON	ATX Power on signal	14	Green

Note. The +12VDC and -12VDC voltages are neither used nor generated by the CPU-1232 module: they are only conveyed on the PC/104-Plus bus (connector J1) and can be used by other devices or modules that are stacked onto the CPU module.

WARNING! IMPROPER CONNECTION OF THE POWER SUPPLY WILL RESULT IN SERIOUS DAMAGE TO THE MODULE.

This application note presupposes that the user will provide a power supply to CPU-1232 connections as described on Table 5.

The following table outlines the pin-out of the Standard ATX female connector with the suggested 18AWG wire color.

Table 6. ATX Power Connections

Pin	Signal	Signal	Pin
11 **11**	+3.3 VDC - Orange(22AWG) 3.3V sense - Brown(22AWG)	+3.3 VDC - Orange	**1**
12	-12 VDC Blue	+3.3 VDC - Orange	**2**
13	Black COM	COM - Black	**3**
14	Green PS-ON	+5 VDC - Red	**4**
15	Black COM	COM - Black	**5**
16	Black COM	+5 VDC - Red	**6**
17	Black COM	COM - Black	**7**
18	White -5 VDC	POK - Gray	**8**
19	Red +5 VDC	+5VSB - Purple	**9**
20	Red +5 VDC	+12 VDC - Yellow	**10**

Chapter 2 SPM Management

The Soft Power Management (SPM) capabilities of the CPU-1232 are integrated into the *Su*per I/O FDC37b782 chipset and for the Wake on LAN also on the RTL8139C Ethernet chip.

The CPU-1232 has the capability to be placed in a low-power operating mode where CPU activity is stopped and power consumption reduced. Operating in this mode is made possible when supplying the CPU-1232 with the power supply architecture described in Table 5.

All wake-up event registers and related logic are battery backed-up to retain the configuration of wake-up events upon a power loss (i.e., Vcc=0V and 5 VSB=0V). The battery can be connected or through the pins 7 (+) and pin 1 (-) of the Multifunction/VGA/Ethernet connector J7. The battery supply voltage must be 3.0 V (minimum 2.4V, maximum 4V).

The low power mode can be activated through software or via a power button, whereas it can be deactivated from either the power button or from one of a number of wake-up events.

This Soft Power Management section covers a few fundamental points:

- Initializing the SPM CPU peripheral to enable wake-up events
- Placing the CPU in a low power mode
- Waiting for wake-up events

SPM SW Initializations

Chapter 3 is dedicated to the description of the *Su*per I/O and Realtek SPM registers. Chapter 4 describes the software programming mode to access previous registers. For a list of detailed examples on programming Wake-up functions, please refer to Chapter 5.

Entering Low Power mode

This chapter describes how to enter the low power mode and which events allow user to wake-up the CPU-1232 from a sleep state.

To reduce power consumption, the CPU should be placed in a low power consumption mode. This may be done in two different ways:

- via External Power Button
- via software

External Power Button

Low power consumption may be achieved by pressing an external power button, which allows a user to place the CPU-1232 in a state where only the +5VSB is supplying power to a part of the *Super I/O* and Ethernet adapter (RTL8139C chip) in a wait-for-event state.

There are two different power buttons the user can use to place the CPU into a low power consumption mode:

ATX Power Button

If the user uses the ATX power button, the user can shutdown the system as a standard ATX PC at any time. This is not an ideal mode to manage the SPM mode because the user application doesn't have any information regarding the power on/off modes.

External Power Button

The external Power Button (PWR_BTN pin 10 of J3 connector) should be connected between pin 10 and 7 of J3 connector to enable the user to power down or up the CPU. This feature may be enabled or disabled by writing proper values on the *Super I/O* registers.

Software

The user can enter into low power mode by writing to the registery through software. This will allow the user to shut the CPU down remotely.

The SPM may be managed by software programming the Software Power Down Registers as described in this document.

Wakeup events

The hardware of the CPU-1232 allows users to manage the Soft Power management modes using the following wake-up events sources:

- External Power Button
- nRinging pin
- Wake on RTC
- Ethernet

All the possible wake-up events could be enabled or disabled by setting Soft Power Enable Registers. The user can also know what event has occurred to turn on the power by reading the Soft Power Status Registers. Note: the status bit is set if a wake-up event occurs, whether or not it is enabled as a wake-up function through the corresponding Soft Power Enable Register. However, only the enabled wake-up functions will turn on power to the system.

ATX Power on signal

The signal that commands an ATX-like power supply is present at pin 12 of the J11 connector (ATX ON pin). This pin presents an active low, open drain signal.

For an ATX power supply, when this signal is held high or left open circuited, inputs of the power rails should not receive current and should be held at a zero potential with respect to ground (except for the secondary supply 5VSB that is always present at the pin 11 of the same J11 connector).

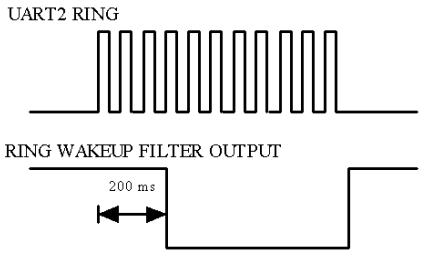
External Power Button PB pin (connector J5-pin 10):

A low signal in the Power Button pin (if enabled) can be used to turn the system on and off from the low power mode. A low level on this pin activates the wake-up functionality.

nRINGING pin (connector J17-pin 1)

This hardware wake-up event from a sleep state is activated with a high signal in this pin. Level should be greater than 3V because this signal is applied to a GATE of a MOSFET, which drives the GP11 pin of the FDC37B782 chip.

An optional filter, if enabled, is provided to prevent glitches to wake-up circuitry and prevent any unnecessary system wake-ups. A wake-up event is activated when the filter receives a signal that produce at least 3 edges in a 200 ms time period, i.e. it detects a pulse train of frequency 15 Hz or higher. The wake-up signal is activated for the duration of the received signal.



This filter circuit is powered by the 5VSB power supply. When this circuit is disabled, it will draw no current. The user can use the nRINGING connector as an External Power Button to Power up the CPU-1232.

In case the user wants to use the nRINGING in conjunction with a push button, connect the button between pin 1 and 2 of J17 pulling up to +5VSB with a 1Kohm resistor pin 1.

In most cases, the user can utilize the External Power Button to manage the power up and down capabilities, leaving the nRINGING connector to manage the Wake–on-Serial Events. Connect pin 1 of J17 to a RS232 serial input pin (e.g. DCD, RX, DSR, CTS and RI).

Please refer to Chapter 5 for a practical example of using the Wake–on-nRINGING functionality.

Wake on RTC

A hardware wake-up event from the sleeping state can be made at a predetermined time with an RTC alarm. Please be careful that the RTC is updated. User should initialize the RTC alarm registers and then place the CPU into Low power consumption mode. When the RTC reaches the RTC alarm count, the CPU will wake up.

Please refer to Chapter 5 for a practical example using the Wake–on-RTC functionality.

Ethernet

The CPU-1232 module includes a Realtek RTL8139C chip to realize Ethernet functionalities. This chip is compliant with ACPI (Rev. 1.0) and PCI Power management (Rev 1.0). The chip monitors the network, looking for a Wake-up Frame, Magic Packet, or a Link change and notifies of the event via the PME# pin. The chip can also be isolated from the PCI bus automatically with the auxiliary power circuit when the PCI bus is in B3 state.

Magic Packet from the network

(Just for CPU-1232 module in mode A): A remote computer can utilize the Magic packet* to wake up the module. Once the module has been enabled for Magic Packet* wake-up and has been put into this state, it scans all incoming packets addressed to the node for a specific data sequence, which indicate to the

controller that this is a Magic Packet* frame. A Magic Packet* frame must also meet the basic requirements: Destination address + Source address + data + CRC The destination address may be the node ID of the receiving station or a multicast address, which includes the broadcast address. The specific sequence consists of 16 duplications of 6 byte ID registers - with no breaks or interrupts. This sequence can be located anywhere within the packet, but must be preceded by a synchronization stream, 6 bytes of FFh. The device will also accept a multicast address, as long as the 16 duplications of the IEEE address match the address of the ID registers. If the Node ID is 11h 22h 33h 44h 55h 66h, then the magic frame' s format is like the following:

Destination address + source address + MISC + FF FF FF FF FF FF + MISC + 11 22 33 44 55 66 + 11 22 33 44 55 66 + 11 22 33 44 55 66 + 11 22 33 44 55 66 + 11 22 33 44 55 66 + 11 22 33 44 55 66 + 11 22 33 44 55 66 + 11 22 33 44 55 66 + 11 22 33 44 55 66 + 11 22 33 44 55 66 + 11 22 33 44 55 66 + 11 22 33 44 55 66 + 11 22 33 44 55 66 + 11 22 33 44 55 66 + 11 22 33 44 55 66 + MISC + CRC

Please refer to Chapter 5 for a practical example of using the Magic Packet functionality.

Chapter 3 SPM REGISTERS

The SPM register model consist of a number of fixed register blocks that perform designated functions. A register block consists of a number of register that perform Status, Enable and Control Functions.

- Status bits are only set through certain defined hardware events
- Unless otherwise noted, Status bits are cleared by writing a HIGH to that bit position, and upon VTR POR. Writing 0 has no effect
- Status bits only generate interrupts, while their associated bit in the enable register is set
- Function bit positions in the status register have the same bit position in the enable register.

Wake-up event configuration is retained by battery backup power.

The following tables report the register of this chipset that may be programmed or read to manage the SPM functionalities.

Table 7. SPM registers – indexed

Index	Function	Default
B0h	Soft Power Enable Register 1	0x00 on VBAT POR
B1h	Soft Power Enable Register 2	0x80 on VBAT POR
B2h	Soft Power Status Register 1	0x00 on VBAT POR
B3h	Soft Power Status Register 2	0x00 on VBAT POR
B8h	Delay 2 Time Set register	0x00 on VBAT POR
C6h	Ring Filter Select	0x00 on VBAT POR
E1h	NRINGING - GP11	0x01 on VBAT POR
F1h	Watch-dog Timer Units	0x00 on VBAT POR or Reset_Drv
F2h	Watch-dog Timer Time-Out Value	0x00 on VBAT POR or Reset_Drv
F3h	Watch-dog timer Configuration	0X00 on VBAT POR or Reset_Drv
E4h	Magic Packet	0x05
F4h	Software Power Down	0x00 Cleared by VTR POR

Table 8. Register B0h Soft Power Enable Register 1

Register B0h Soft Power Enable Register 1	
Bit	Description
7..0	The following bits enable the wake-up event. When enabled, these bits allow their corresponding function to turn on power to the system. 1 = ENABLED 0 = DISABLED Bit[0] Reserved (0 default) Bit[1] Reserved Bit[2] Reserved (0 default) Bit[3] Reserved (0 default) Bit[4] Reserved (0 default) Bit[5] Reserved (0 default) Bit[6] Reserved Bit[7] RTC Alarm (Watchdog)

Table 9. *B1h Soft Power Enable Register 2*

Register B1h Soft Power Enable Register 2	
Bit	**Description**
7..0	The following bits enable the wake-up event. When enabled, these bits allow their corresponding function to turn on power to the system. 1 = ENABLED 0 = DISABLED Bit[0] Reserved (0 default) Bit[1] Reserved Bit[2] Reserved Bit[3] RING Enable bit "RING_EN" Bit[4] Reserved Bit[5] Reserved (0 default) Bit[6] Reserved Bit[7] OFF_EN: After power up, this bit defaults to 1, i.e., enabled. This bit allows the software to enable or disable the button control of power off.

Table 10. B2h Soft Power Status Register 1

Register B2h Soft Power Status Register 1	
Bit	**Description**
0..7	The following bits are the status for the wake-up event. These indicate which of the enabled wake-up functions caused the power up. 1 = Occured 0 = Did not occur since last cleared The following signals are latched to detect and hold the soft power event (Type 1) Bit[0] Reserved Bit[1] Reserved Bit[2..5] Reserved Bit[6] Magic Packet Bit[7] RTC Alarm; status of the RTC Alarm internal signal. Cleared by a read of the status register.

Table 11. B3h Soft Power Status Register 2

Register B3h Soft Power Status Register 2	
Bit	**Description**
0..1	Reserved
3	The following bits are the status for the wake-up event. These indicate which of the enabled wake-up functions caused the power up. 1 = Occured 0 = Did not occur since last cleared The following signals are latched to detect and hold the soft power event Bit[3] RING Status bit "RING_STS"; Latched, cleared on read 0 = nRING input did not occur. 1 = Ring indicator input occured on the nRING pin and, if enabled, cause the wake-up (activate nPowerOn)
4..7	Reserved

Table 12. B8h Delay 2 Time Set register

Register *B8h Delay 2 Time Set register*	
Bit	**Description**
0..7	This register is used to set Delay 2 (for Soft Power Management) to a value from 500 msec to 32 sec. The default value is 500msec. Note: this delay is started if OFF_EN is enabled and OFF_DLY was set and a Button Input comes in. Bits[5:0] The value of these bits correspond to the delay time as follows: 000000= 500msec min to 510msec max 000001= 1sec min to 1.01sec max 000010= 1.5sec min to 1.51sec max 000011= 2sec min to 2.01sec max ... 111111 = 32sec min to 32.01sec max Bits[7:6] Reserved

Table 13. Register C6h Ring Filter Select Register

Register C6h Ring Filter Select Register	
Bit	**Description**
0..2	This register is used to select the operation of the ring indicator on the nRI1, nRI2 and nRING pins. Bit[0]: 1=Enables detection of pulse train of frequency 15Hz or higher for 200msec and generate an active low pulse for its duration to use as the ring indicator function on nRING pin. The leading high-to-low edge is the trigger for the ring indication. 0=Ring indicate function is high-to-low transition on the nRING pin. Bit[1]: 1=Enables detection of pulse train of frequency 15Hz or higher and generate an active low pulse for its duration to use for 200msec as the ring indicator function on nRI1 pin. The leading high-to-low edge is the trigger for the ring indication. 0=Ring indicate function is high-to-low transition on the nRI1 pin. Bit[2]: 1=Enables detection of pulse train of frequency 15Hz or higher and generate an active low pulse for its duration to use for 200msec as the ring indicator function on nRI2 pin. The leading high-to-low edge is the trigger for the ring indication. 0=Ring indicate function is high-to-low transition on the nRI2 pin.
3..7	Bits[7:3] Reserved

Table 14. Register E1h nRINGIN (GP11)

Register E1h nRINGIN GP11	
Bit	**Description**
0..7	Must be set to 09h

Table 15. Register E4h Magic Packet

Register E4h Magic Packet	
Bit	**Description**
0..7	Must be set to 05h

Table 16. Register F1h WDT_Units

Register F1h WDT_Units	
Bit	**Description**
0..7	Watch Dog Timer Units Bits[6:0] Reserved, = 00000 Bit[7] WDT Time-out Value Units Select = 0 Minutes (default) = 1 Seconds Note: if the logical device's activate bit is not set, bits 0 and 1 have no effect.

Table 17. Register F2h WDT_VAL

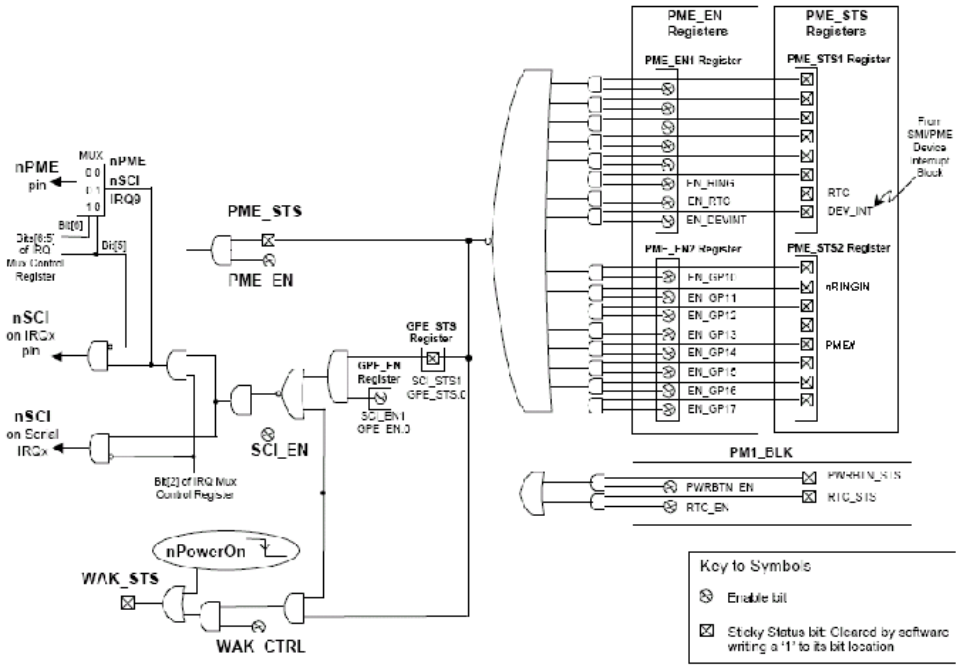
Register F2h WDT_VAL	
Bit	**Description**
0..7	Watch-dog Timer Time-out Value Binary coded, units = minutes(default) or seconds, selectable via Bit[7] of Reg 0xF1, LD 8. 0x00 Time out disabled 0x01 Time-out = 1 minute/second ..... 0xFF Time-out = 255 minutes/seconds

Table 18. Register F4h Software Power Down

Register F4h Software Power Down	
Bit	Description
7	SPOFF: this is used to force a software power down . this bit is self clearing
6	Reserved

Warning: the reserved bits must not be modified.

The following image describe in a graphically format, the relationship between nRINGIN, PME# signals and *Super I/O* registers.



Refer to the *Super I/O* FDC37b782 datasheet to the following table for a quick signal reference between GPIO of *Super I/O* pins and CPU-1232 signals:

Table 19. Super I/O versus CPU-1232 signal correspondance

Super I/O PIN	*Super I/O* Signal	CPU-1232 SIGNAL
78	RING_GP11	RINGIN#
81	RXIR_GP14	PME# - Realteck RTL8139C Output

For further detailed information regarding the *Super I/O* FDC37b782 chip, please refer to the component manufacturer's datasheet.

RTC Real Time Clock registers

The Super IO FDC37b782 contains a standard PC Real time clock architecture accessible at the following addresses:

Table 20. Super I/O RTC ISA I/O Address Map

ISA ADDRESS*	BLOCK	FUNCTION
0x70 (R/W)	RTC	Address Register
0x71 (R/W)	RTC	Data Register
Base*	RTC Bank 1	Address Register
Base* + 1	RTC Bank 1	Data Register

The following table contains information regarding the RTC registers.

Table 21. Super I/O RTC Registers

ADDRESS REGISTER	TYPE REGISTER	FUNCTION
0	R/W	Register 0: Seconds
1	R/W	Register 1: Seconds Alarm
2	R/W	Register 2: Minutes
3	R/W	Register 3: Minutes Alarm
4	R/W	Register 4: Hours
5	R/W	Register 5: Hours Alarm
6	R/W	Register 6: Day of Week
7	R/W	Register 7: Date of Month
8	R/W	Register 8: Month
9	R/W	Register 9: Year
A	R/W	Register A:
B	R/W	Register B: (Bit 0 is Read Only)
C	R	Register C:
D	R/W	Register D:VRT and Day of Month Alarm
0E-7Ch	R/W	Register E-7C: General Purpose
7Dh	R/W	Register 7D: Century Byte
7Eh	R/W	Register 7E: Control Register 1
7Fh	R/W	Register 7F:General Purpose

RTL8139C Power Management registers

To use the Wake-on-LAN functionality, the user needs to manage the Realtek RTL8139C Ethernet chip.. After a reset, the Ethernet adapter loads the default parameters stored in EEPROM. These parameters can be modified by the user with the RSET8139.exe software utility contained into the Eurotech Driver & Manual CDROM.

The default values programmed by the factory using are listed on Table 22:

Table 22. Realtek RTL8139C Setup New Configuration Menu default values

Field	Value
Medium Type	Autodetect
Boot ROM size	No Boot ROM
Flow Control	TX Disable, Rx Disable
Wake On Lan	ENABLE
Link Change	DISABLE
Lan Wake Signal	Active high

For a detailed list of all Realtek RTL8139C chip registers, please refer to the component datasheet.

To enable the Wake–On-LAN functionality using the default Eurotech EEPROM setting, the user should write to the PMCSR register described in Table 23.

Table 23. Realtek RTL8139C PCI Configuration Space

No	Name	Type	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
54h	PMCSR	R	0	0	0	0	0	0	Power State	
		W	-	-	-	-	-	-	Power State	
55h		R	PME_ Status	-	-	-	-	-	-	PME_En
		W	PME_ Status	-	-	-	-	-	-	PME_En

The RTL8139C provides the following set of operational registers mapped into PCI memory space or I/O:

Table 24. Realtek RTL8139C PCI memory or I/O space operational registers

Offset	Type	Tag	Description
0000h	R/W	IDR0	ID Register0, the ID register 0-5 are only permitted to read/write by 4-bye access.
0001h	R/W	IDR1	ID Register1
0002h	R/W	IDR2	ID Register2
0003h	R/W	IDR3	ID Register3
0004h	R/W	IDR4	ID Register4
0005h	R/W	IDR5	ID Register5

This information is useful when looking for the MAC address of the CPU-1232.

Chapter 4 Configuration

In order to set the various options of the SPM, the user has to set the proper registers. The SPM registers are I/O mapped at the address 03F0h. Its registers (Table 25) are accessed by writing their relative index in the INDEX PORT (I/O address 03F0h), which are then read-modify-write to the DATA PORT (I/O address 03F1h).

Table 25. Configurations registers – I/O mapped

Address	Function	Type
3F0h	INDEX PORT	Write
3F1h	DATA PORT	Read/write

To program or read the configuration registers, the following sequence must be followed:

1. Enter Configuration State and select the Watchdog device
2. Select the right function
3. Exit Configuration State

The INDEX and DATA PORT are effective only when the timer is Configuration State.

Enter Configuration State (Unlock Chip)

To enter into the Configuration State, write <55h> to the INDEX PORT. After that, select the SPM device writing <07h> to the INDEX PORT and <08h> to DATA PORT.

Configuration sequence

Write the index of the desired SPM register to the INDEX PORT and then write or read the configuration register trough DATA PORT.

Exit Configuration State (Lock Chip)

To exit the Configuration State write AAh to the INDEX PORT.

Chapter 5 Software Examples

This section is useful to demonstrate how to write code to control the SPM modes. The examples are developed using the DOS O.S., referring to the DEBUG.EXE program. The blue sentence are comments.

Wake on nRINGING

The following is an example of a configuration procedure that enables an nRING wake-up event.Make proper power connections as described in Table 5 and connect the J17 pin 1 connector to an RS232 serial input pin (e.g. DCD, RX, DSR, CTS and RI). In case you use the RI serial pin, a modem must be connected to the serial port to generate the RINGING signals, in other cases, RX pin data on serial can wake up the CPU.

```
C:\>Debug
;Enter Configuration Mode
-o 3F0 55                    ; Chip unlocked
-o 3F0 07                    ;Select SPM Registers
-o 3F1 08

;Configure a Register
-o 3F0 B1                    ;Select Soft Power Enable Register 1
-o 3F1 88                    ;Enable nRING Wake up event

-o 3F0 B3                    ;Reset Power Status Register (if not you couldn't place the CPU in LPM)
-i 3F1
-i 3F1

-o 3F0 E1                    ; Configure GP11 pin of FDC37B782 as nRING input
-o 3F1 09

-o 3F0 F4                    ; Place the CPU into Low Power Mode
-o 3F1 80
;The CPU is now sleeping!! So you are able to Lock the Chip first to sleep it. After powering up the CPU with a wake-up event the chipset is Locked!
```

To verify the wake-up functionality, the user should try to send data on the serial port from a host computer and verify that the CPU starts.

Wake on RTC

The following is an example of configuration procedure to enable an RTC wake-up event.

In this example, provide (by software initialization) the RTC date and time registers as 0:0:0, and then program the RTC alarm register to wake up the CPU module after a minute (0:1:0).
After the CPU has been placed in sleep mode, the Wake-on-signal appears after 1 minute.

User can also initialize the Date and Time through the BIOS, programming by software only the RTC Alarm register.

Ensure proper power connections, as described in Table 5.

```
C:\>Debug
;Configure RTC Registers
- O 70 B                    ; inhibits any update cycle and then clears the UIP status bit
- O 71 82
;Program the Seconds Register 0
- O 70 0
- O 71 0
;Program the Seconds Alarm Register 1
- O 70 1
- O 71 0
;Program the Minutes Register 2
- O 70 2
- O 71 0
;Program the Minutes Alarm Register 3
- O 70 3
- O 71 1
;Program the Hours Register 4
- O 70 4
- O 71 1
;Program the Hours Alarm Register 5
- O 70 5
- O 71 1

- O 70 B                    ; enable update cycle
- O 71 22

;Enter Configuration Mode
- O 3F0 55                  ; Chip unlocked
- O 3F0 07                  ;Select SPM Registers
- O 3F1 08

- O 3F0 B2                  ;Reset Power Status Register (if not you couldn't place the CPU in LPM)
- I 3F1
- I 3F1

- O 3F0 B0                  ;Select Soft Power Enable Register 1
- O 3F1 80                  ;Enable SP_RTC Alarm: RTC Alarm

- O 3F0 F4                  ; Place the CPU into Low Power Mode
- O 3F1 80
; The CPU is now sleeping!! You are not able to Lock the Chip first to sleep it. After powering up the CPU with a wake-up
event the chipset is unlocked!
```

Magic Packet

The following is an example of configuration procedure enabling a Wake-On-LAN wake-up event.

To begin, the user should verify that the Network peripheral is enabled from the BIOS; you will need to detect the MAC address of the CPU-1232 Ethernet adapter. This may be done using the RSET8139.exe SW utility contained into the Eurotech Manual & Drivers CDROM.

The user will have to configure the register of the Realtek Chip and the *Super I/O*, as described in the following example to enable the Wake–On-Lan functionality.

C:\>Bustrek

-pww 0 e 0 54 8101 *; Write a Word in the 54h Register into the PCI Configuration Space to enable PME status, PMEen, Power State*

After a Magic Packed has occurred the PME# pin assume a low logic level, this level is retained until a new write is done on register 54h with the same previous command.

C:\>Debug
;Enter Configuration Mode
-o 3F0 55 *; Chip unlocked*
-o 3F0 07 *;Select SPM Registers*
-o 3F1 08

-o 3F0 B2 *;Reset Power Status Register (if not you couldn't place the CPU in LPM)*
-i 3F1
-i 3F1

;Configure a Register
-o 3F0 E4 *; Configure GP14 pin of FDC37B782 as PME (Magic Packet) input, Invertedand Group Interrupt*
-o 3F1 07 *;Enable Magic Packet Wake up event*

-o 3F0 BO *;Select Soft Power Enable Register 0*
-o 3F1 10 *;Enable SP_GPINT1: Group Interrupt 1 (Magic Packet Wake up event)*

-o 3F0 F4 ; Place the CPU into Low Power Mode
-o 3F1 80
;The CPU is now sleeping!! So you are not able to Lock the Chip first to sleep it. After powering up the CPU with a wake-up event the chipset is unlocked!

The CPU-1232 is now in a low power consumption state, waiting for the Magic Packet event to wake-up.

To verify the Wake–On-LAN functionality now you will need to send a Magic Packet to the CPU-1232 via Ethernet. This may be done using specific software, for example under Linux you can use the EtherWake program with the following syntax:

Etherwake -i ethxx XX:XX:XX:XX:XX:XX

Where ethxx is the host Ethernet adapter with the CPU-1232 connected, the XX:XX:XX:XX:XX:XX field is the MAC address of the CPU-1232. The program sends a magic packet stream over the Ethernet cable compliant to the AMD magic packet specification.

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Chapter 6 CPU-1232 Power Consumption

The main goal of Soft Power Management is to reduce CPU power consumption when not needed.
This brief chapter compares the power consumption of a CPU-1232 module with a CPU clock frequency of 266MHz and 128MB RAM, running in standard mode and low power mode.

The following tables show the differences of power consumption between standard power management and soft power management in the various configurations.

Table 26. Soft power management consumption with the module at

Clock	266 MHz
128 Mbyte	5V @ 1000mA

Table 27. Soft power management consumption with the module in the low power mode

Clock	266 MHz
128 Mbyte	5VSB @ 100mA

In these tables, the reader will note that the energy saved with low power mode is very high. It is further increased by taking off the network circuitry from the low power mode.

Related Documents

For further information about the SUPER I/O device *SMSC FDC 37B782 and Realtek RTL8139C please refer to their technical Datasheets.*