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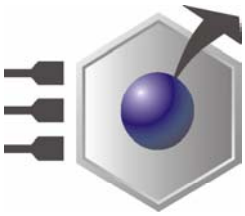

EuroTecH

An0014

GX1-CS5530A: ISA clock

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Conventions

The following table lists conventions used throughout this guide.

Icon	Notice Type	Description
	Information note	Important features or instructions
	Warning	Information to alert you to potential damage to a program, system or device or potential personal injury

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Introduction

With CPU's based on the Geode GX1 chipset and its companion CS5530A, the ISA bus clock is derived from the PCI clock by division.

The CPU's that are affected by this application note are:

- CPU-1232
- CPU-1432

Normally the PCI clock has a frequency of 33.3MHz and the BIOS has a division setting of four, in this way the ISA clock frequency is 8.3MHz.

This application note describes how to modify the ISA clock timing, and describes the risks of going outside of the ISA standards.

Other information can be found in the following documentation:

- The individual CPU user manuals
- The individual CPU Application Notes
- Cs5530A Chipset Manual
  - Geode™ CS5530A I/O Companion Multi-Function South Bridge
- PCI Hardware and Software Architecture and Design di E.Solari
  - Printed by AnnaBooks ISBN 092939259-0

Altering the ISA clock frequency

Within the CPU123X / CPU1432 the internal PCI peripheral chipset are addressed on Bus 0, Device 12h, in particular interest is the PCI/ISA bridge, Function 0.

We are interested in the first three bits of the PCI configuration register:

- Bus 0, Device 12h, function 0, Offset 50h

The following table shows the definition of these 3 bits:

Bit	Definition
2:0	000: Reserved 001: Divide by two 010: Divide by three 011: Divide by four 100: Divide by five 101: Divide by six 110: Divide by seven 111: Divide by eight

Normally the divider is set to the standard value of 4, this gives a clock value of 8.33MHz.

With this value the pulse width of the control signal “IOread#” is approximately 540ns.

The value of this divider can be modified to perform the bus characteristics.

For example:

- With the divider value set to 3 you will obtain a clock of 11.1MHz with the pulse width of the control signal IORead# around 400ns.
- With the divider value set to 2 you will obtain a clock frequency of 16.7MHz with the pulse width of the control signal IORead# around 268ns.

Important

It is possible to modify the ISA bus clock by programming the registers and modifying the timing characteristics of the control signals.
This operation must be accurately verified because reprogram the entire ISA Bus timings without any warranty of functionality.
The operator must verify the proper functionality also in conjunction with the add-on boards and verify the CPU thermal characteristics with the new clock operating ranges.

Examples

In the same directory of this Application note you will find an example program for modifying the clock divider (these are contained in the file “AN0014 Files.zip”).

The files are:

File Name	Description
AN14.c	Source code for AN14.exe
SP_PCI.h	Header of the functions to access the PCI configuration register
SP_PCI.c	Functions to access the PCI configuration register
AN14.exe	Compiled example program
cwsdpmi.exe	DPMI provider
copying	GNU General PUBLIC LICENSE

The software was compiled using the GNU compiler version 2.95.3

If you do not have a DPMI server, first launch the CWSDPMI.exe program and then the AN14.exe

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