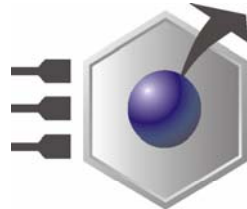


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**CPU-7630: I/O Memory Map**

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## ABOUT THIS MANUAL

This application note contains information regarding the I/O Memory map for the CPU-7630



Via J. Linussio 1  
33020 AMARO (UD)  
ITALY

Phone: +39 0433 485 411  
Fax: +39 0433 485 499

Web: [www.eurotech.it](http://www.eurotech.it)  
E-mail: [sales@eurotech.it](mailto:sales@eurotech.it)

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## Conventions

The following table lists conventions used throughout this guide.

Icon	Notice Type	Description
	<b>Information note</b>	Important features or instructions
	<b>Warning</b>	Information to alert you to potential damage to a program, system or device or potential personal injury

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## CPU-7630 I/O Port Map

On CPU-7630 the I/O address space from E0h to ECh is used for internal glue logic

These registers can be accessed with simple I/O operations.

However only the bits 0, 1 & 2 are useful, writing or reading to bits 4 thru 7 will make an undefined result.

The following tables give a brief description of each of these registers.

### General Board Status, Control and Revision registers

#### I/O Port E0h, E2598\_STATUS\_Register\_0

Reset value: 0XX

Bit	Mode	Name	Description
2:1	Not Applicable	Reserved	
0	Read only	INVEE_EXTBIOS_STATUS	0: Jumper Ext BIOS or Invalid Setup inserted 1: Jumper Ext BIOS or Invalid Setup left open

#### I/O Port E1h, E2598\_Watchdog\_configuration\_register

Reset value: 000

Bit	Mode	Name	Description
2	Read / Write	PB_NMI_EN	Enable NMI pushbutton:  0: Pushbutton disabled (Default at reset) 1: Pushbutton causes NMI
1	Read / Write	WD_NMI	Choose event at timeout:  0: Watchdog timeout triggers reset (Default at reset) 1: Watchdog timeout triggers NMI
0	Read / Write	WD_RES	Enable Watchdog circuit "WD"  0: Watchdog WD disable (Default at reset) 1: Watchdog WD enable

### I/O Port E2h, E2598\_FlashCTRL

Reset value: 00x

Bit	Mode	Name	Description
2	Read / Write	VPPEN	Enable VPP to Flash device:  0: VPP disabled (Default at reset) 1: VPP applied to flash device
1	Read / Write	E2598_FLASHCTRL	Set flash to reset / power down mode  0: Normal behavior (Default at reset) 1: Reset / Power down
0	Not Applicable	Reserved	

### I/O Port E3h, E2598\_CNFG\_BANK

Reset value: 000

Bit	Mode	Name	Description
2:0	Read / Write	E2598_CNFG_BANK	Choose the device present on SSD socket or the device decoded in E8000h window (32k wide)  000: None device selected 001: Flash BIOS on E8000h

### I/O Port E4h (Read), E2598\_REVL

Reset Value: Not Applicable

Bit	Mode	Name	Description
2:0	Read only	E2598_REVL (0:2)	Low byte of programmable revision level

### I/O Port E4h (Write), E2598\_ADDBL

Reset value: 000

Bit	Mode	Name	Description
2:0	Write only	E2598_ADDBL	Page address (ADDB16:14) for Flash

### I/O Port E5h (Read), E2598\_REVH

Reset Value: Not Applicable

Bit	Mode	Name	Description
2:0	Read only	E2598_REVH (0:2)	High byte of programmable revision level



## I/O Port E5h (Write), E2598\_ADDBH

Reset Value: 000

Bit	Mode	Name	Description
2:0	Write only	E2598_ADDBH	Page address (ADDB19:17) for Flash

## Serial Control Registers

### I/O Port E6h, E2598\_SERIAL\_CONTROL0

Reset Value: 000

Bit	Mode	Name	Description
2	Not Applicable	Not Applicable	
1:0	Read / Write	E2598_SERIAL_CONTROL0	Setting for first serial port (J5 connector) 00: Disabled 01: RS232 mode 10: RS422 mode 11: RS485 mode

### I/O Port E7h, E2598\_SERIAL\_CONTROL1

Reset Value: 000

Bit	Mode	Name	Description
2:1	Not Applicable	Not Applicable	
0	Read / Write	E2598_SERIAL_CONTROL1	Setting for second serial port on J6 connector 00: Disabled 01: RS232 mode 10: RS422 mode 11: RS485 mode

## External devices related registers

### I/O Port E8h, E2598\_Watchdog\_Index\_Register

Reset Value: xxx

Bit	Mode	Name	Description
2:0	Read / Write	E2598_WDINDEX	Watchdog circuit "WDA" index register

### I/O Port E9h, E2598\_Watchdog\_Data\_Register

Reset value: xxx

Bit	Mode	Name	Description
2:0	Read / Write	E2598_WDDATA	Watchdog circuit "WDA" data register

### I/O Port ECh, E2598\_Timer\_IRQ\_Register

Reset value: x10

Bit	Mode	Name	Description
2	Read / Write	E2598_TIMER0_IRQ	Enable IRQ on Timer 0 active: 0: No IRQ 1: IRQ active if Timer 0 output at high level
1	Read / Write	E2598_TIMER1_IRQ	Enable IRQ on Timer 1 active: 0: No IRQ 1: IRQ active if Timer 1 output at high level
0	Read / Write	E2598_TIMER2_IRQ	Enable IRQ on Timer 2 active: 0: No IRQ 1: IRQ active if Timer 2 output at high level

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## Timer Registers

The 8254 compatible timer has 4 registers as described below

<b>Index</b>	<b>Register name</b>
<b>120h</b>	Command
<b>121h</b>	Timer 0
<b>122h</b>	Timer 1
<b>123h</b>	Timer 2

SuperIO Registers

<b>Index</b>	<b>Register name</b>
<b>370h</b>	Index
<b>371h</b>	Data
<b>EAh</b>	Runtime Index
<b>EBh</b>	Runtime Data

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## Related Documents

For further information on the CPU-7630 please refer to the following documentation:

- CPU-7630, User Manual.

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## Where to find us

### **Eurotech S.p.A.**

Via Jacopo Linussio, 1 - 33020 Amaro (UD) ITALY  
Tel. +39 0433 485411 - Fax +39 0433 485499

[Welcome@eurotech.it](mailto:Welcome@eurotech.it)

[www.eurotech.it](http://www.eurotech.it)